MAGNETIC CORES AND THEIR APPLICATION TO D. C. COMPUTER REGISTERS

THEODORE SABOE BLY

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by

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Submitted in partial fulfillment
of the requirements
for the degree of
MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

United States Naval Postgraduate School
Monterey, California

1955

This work is accepted as fulfilling
the thesis requirements for the degree of
MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

from the
United States Naval Postgraduate School

PREFACE

Computer development has grown by leaps and bounds in recent years, from a start with the Oriental abacus to the present day giant brains which occupy thousands of square feet, employ thousands of vacuum tubes, crystal diodes and other components. The battle has been toward less costly, more effective, efficient and versatile machines, with heaviest emphasis perhaps placed on reliability. One of the leading causes of breakdown in reliability has been the vacuum tube due both to its own construction and to the heat generated by the tube in operation.

This paper deals with the magnetic-core which has more recently shown promise as a substitute for the vacuum tube in limited applications. An investigation of the operating characteristics of magnetic-cores was conducted toward a study of their use in the shift registers of a digital computer, in particular, a d.c. or NRZ computer. It is believed that the use of magnetic-core units in such an application would be highly beneficial from both an economical and a reliability point of view.

The writer wishes to thank Professor Cotton of the U. S. Naval Postgraduate School for his assistance and suggestions in this project and Mr. Royal E. Howes of The National Cash Register Company, Electronics Division for his patient assistance

and much tutoring throughout the time spent at National Cash Register Company in conducting the investigation and study.

TABLE OF CONTENTS

TABLE OF SYMBOLS AND ABBREVIATIONS

B_R	Residual flux, or remanence
H_c	Coercive force
H_M	Maximum applied magnetizing force
H_o	Threshhold field, magnetizing force, for irreversible domain wall motion
NRZ	Non-return-to-zero, or d.c. coupled, principle of computer design
ONE	Binary digit
RZ	Return to zero, or a.c. coupled, principle of computer design
S_w	Switching Coefficiend
r	Switching Time
ZERO	Binary digit

CHAPTER I

INTRODUCTION

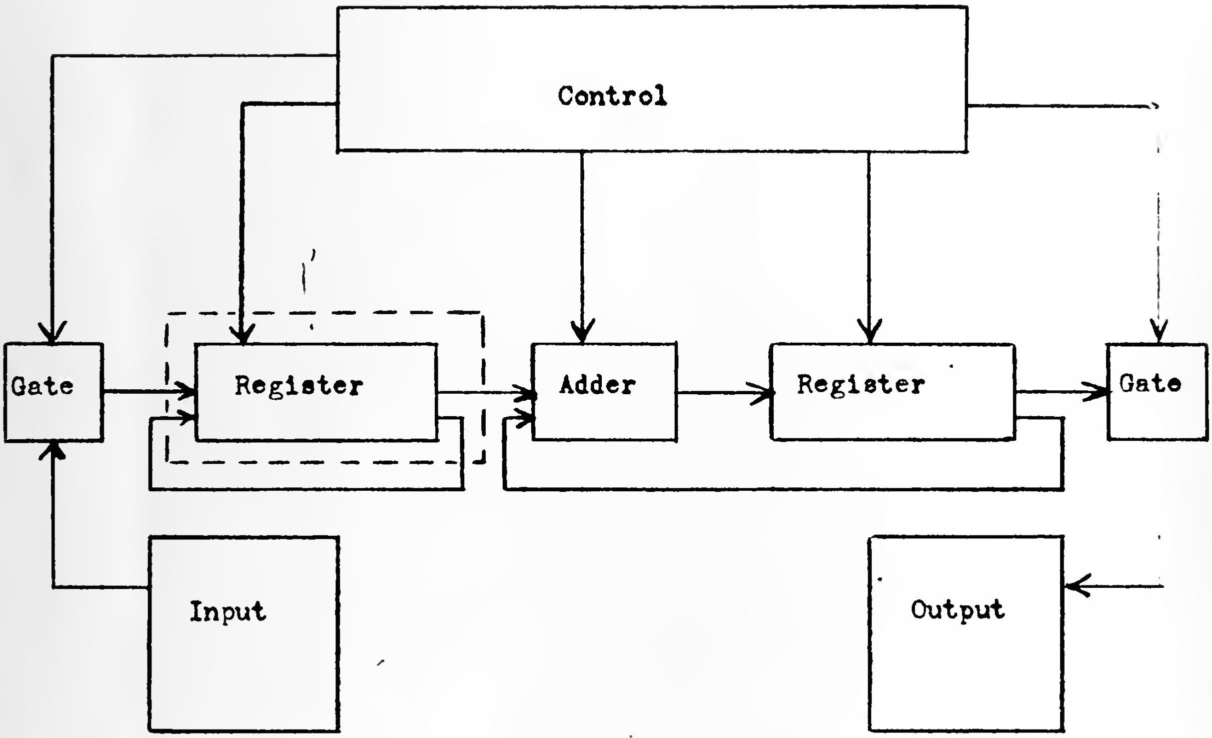
Magnetic cores have become a recognized component part of digital computers, primarily in the random access main memories as used, for example at MIT in the Whirlwind Computer, at RCA as a development project and in the Rand Computer in Santa Monica, California. In each case, magnetic cores have also served as the switches to gain access to the desired portion of the memory. In these applications, the magnetic cores are performing satisfactorily.

However, the use of magnetic cores in stepping or shift registers has not as yet reached this state of acceptance in the computer field, to the writer's knowledge, in spite of the fact that the first applications considered were in the field of registers. The reasons for the lack of wide acceptance or use may have been the cost of the core units, the lack of specific design procedures, or perhaps lack of such outstanding advantages over existing methods as are obtained in the case of the magnetic core random access memories. However, suitable commercial register units have recently made their appearance on the market and are being manufactured of such quality and quantity that at present they can successfully compete with vacuum tube flip-flop stages, and in the future should offer distinct advantages from the points of view of cost and reliability.

This paper, then, deals with a study of the suitability

of magnetic core registers for use in a d.c. coupled digital computer. The d.c. coupled system, often called the non-return-to-zero, or NRZ system, is based on the principle of representing binary information, that is, ONE to ZERO, by two distinct voltage levels, for example: 125 volts represents ONE and 100 volts represents ZERO in a typical case. The voltages in this example are available directly from the plates of a flip-flop in a machine based on this system. The a.c. coupled, or return-to-zero, system represents the information content, electrically, by a pulse or no-pulse, and is more commonly employed in high-speed computers. Certain components operate on one or the other of these principles due to their inherent characteristics and cannot, with ease, be made to operate in the other way. The magnetic core is one of these, since it, as do all transformers, operates on the RZ principle. The problem discussed in this paper is, therefore, the coupling of an RZ system into a machine based on the NRZ techniques, along with the study of the operating characteristics, of the magnetic cores themselves, which make the cores adaptable to computer register applications.

The writer was fortunate in being permitted to conduct a large part of this work in and with the facilities of the National Cash Register Company, Electronics Division, Hawthorne, California. Portions of the work are thus based on the specific type of machine manufactured by that concern, that is, a general purpose,



Typical General Computer System

Figure 1

moderate speed, digital computer based on the NRZ or d.c. coupled form of logic, operating solely in a serial manner. Serial operation only is considered because the circuitry for parallel operation of core units would differ considerably from that for serial operation and the different requirements for a parallel system would be, and have been, the subject of separate study.

A block diagram of a portion of a simple computer is shown in Figure 1. The unit under study for this paper is enclosed in a dashed-line block. An existing register is described in Chapter VI and is used to indicate the input, output and performance requirements of a typical register. The application of a magnetic core register to meet, satisfactorily, the same requirements is dealt with in Chapter VII. A brief history of computer registers and magnetic core usage is discussed in Chapters II and III with a study of the theoretical behavior and structure of magnetic cores. This is followed in Chapters IV and V by a description of the equipment used and of the observations made in checking the performance of commercially available magnetic core register units.

The writer believes that there are definite advantages to be gained in using magnetic core register systems in the computers now being produced as summarized in Chapter VIII.

CHAPTER II

BASIC CONCEPTS

1. Background

Data manipulation is, of necessity, a primary part of any calculation, whether this calculation is carried out long hand, mentally, on a slide rule or by a computer. And to arrive at new results, this manipulation invariably requires the combination in some way of two or more factors, in turn, requiring that each of the factors be "registered" in preparation for the manipulation. This "registering" is carried out, in long hand by writing the factors down, in mental calculation by relying on the memory to retain the factors separately, on a slide rule by use of indicies and the slide, and in a computer by use of registers or delay lines. The method used in the computer, and more specifically, the digital computer, is the subject of this paper.

The main memory of the computer is filled with information either by the programmer or from the results of interim calculations by the computer. The main memory then acts as the source of the factors required for later calculations, and as these factors are called out of memory, they are retained by the register until all necessary factors are ready to proceed with the individual calculation. Thus it can be seen that the register is a type of delay line, and, indeed, delay lines of various sorts have been used as registers, and the the two terms are often

used interchangeably.

A brief discussion of some of the devices used as registers follows with the understanding that the data, with which they are used, is of the binary type and is in the form of a "pulse" or "no pulse" of voltage.

(a) Electronic devices consist, in one form, of flip-flop stages which assume either of two steady states to represent the two information forms. The stages are arranged in series so that when information is fed into or taken out of the register it passes from one stage to the next and appears in its original form at the output, and can be combined with other information in performing the desired calculation. Disadvantages are unreliability, power requirements, heating and size.

(b) Acoustical Delay Lines, of which the mercury delay line is representative, consist of a column of mercury with an acoustic transducer at each end. Information is converted to suitable form, transmitted into the medium at one end of the delay line and is received at the other end after a period of time depending on the characteristics of the medium. The information must then be reconverted to its original form for combination with other information. Disadvantages are temperature effects on the delay, size of delay line and required circuitry and temperature control equipment.

(c) Mechanical Devices, such as relays, use the "make" or

"break" states to indicate the information content. Disadvantages are cost, size, slow speed and unreliability.

(d) Magnetic devices take the form of either magnetic recording, or magnetic cores. Of these, the latter is the subject of this paper and the former will also be discussed in some detail in a comparison of these two magnetic systems.

This, by no means, exhausts the register or delay line techniques but is merely indicative of some of the methods now in use. It is obvious that a useable system must have a high degree of reliability, and a low signal-to-noise ratio such that the information appearing at the output is exactly the same information that was put into the register. In addition, desirable factors are low heat generation (both internal and that radiated to nearby components), low power requirements, low cost, flexibility, small size and compatability with the rest of the computer design in voltage requirements, speed and input/output signal waveforms.

2. Square Loop Magnetic Core History.

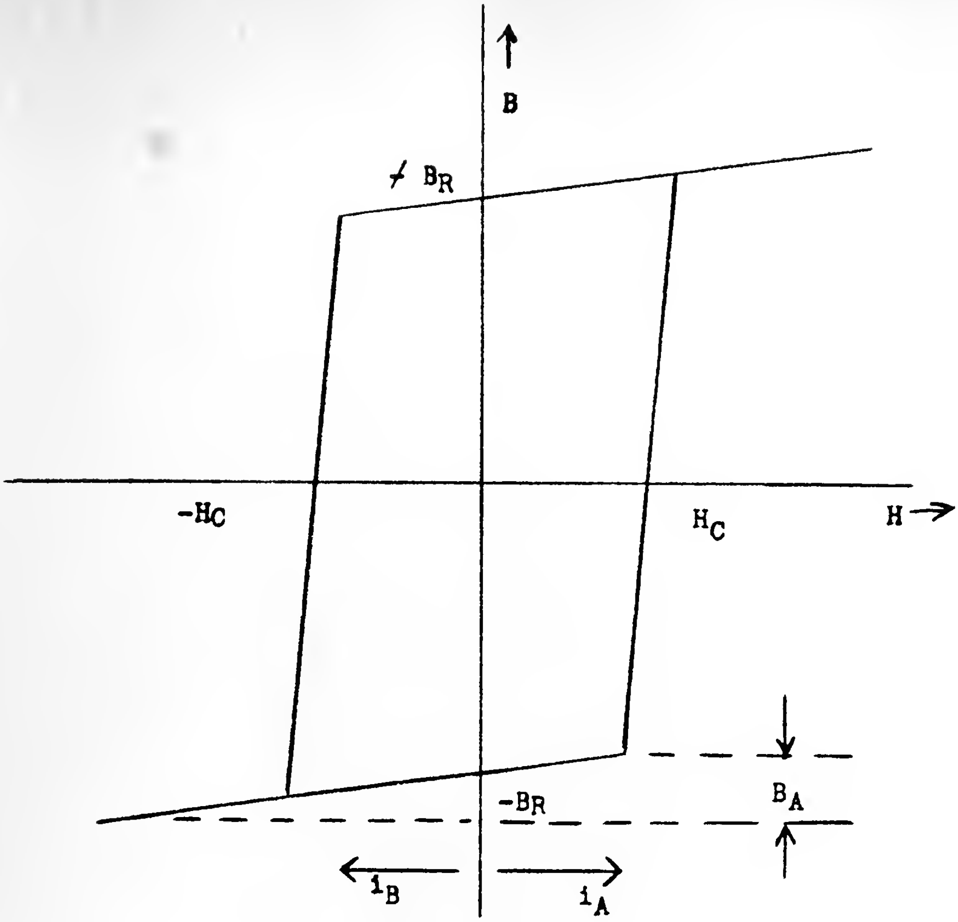
Study of the square-loop ferromagnetic core materials as a bistable element in computer circuits was started about 1948 by Wang [22,23,24] at the Harvard Computation Laboratory and about 1950 by J. W. Forrester [4] at the Whirlwind computer project at M I T and by J. A. Rajchman [16, 17] at RCA Laboratories in connection with computer main memory systems.

Analysis of the core performance was extremely difficult and involved many approximations due to the double-valued non-linear nature of the hysteresis loop [14,21]. Further study of core

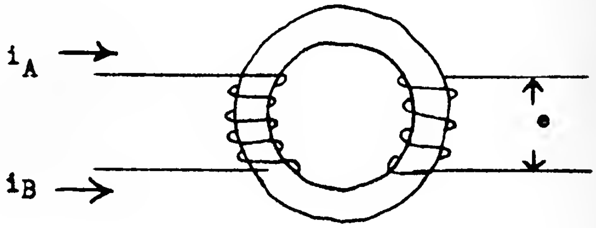
performance proceeded in two not entirely separate directions, one, based on experimental results, refined the existing approximations and based empirical expressions on further assumptions [7,14,18,20,21,23,24], while the other proceeded toward the physical explanation through domain wall motion theory and studies [9,11,15,25]. The latter is beyond the scope of this author's work except in the most basic form, while the former has been depended on considerably and yet does not furnish as complete an understanding as desired on many points. The empirical results do, however, give positive direction to any further experimental work.

3. Brief Description of Core Operation

The magnetic cores of interest in the present application operate in much the same way as a vacuum tube flip-flop circuit in that they are bistable elements and must be triggered in order to shift from one steady state to the other. Figure 2a represents an idealized hysteresis loop of such a ferromagnetic core and figure 2b is a core with a single input winding, through which a current of either polarity may be passed, and a single output winding. Assume that the previous magnetic history has left the core magnetized such that the remanant flux is $-B_R$. An applied current of polarity i_B of such magnitude that the magnetizing force H exceeds H_c, the coersive force, will then cause a flux change of $-B_A$, while an applied current of polarity i_A will cause



2 (a)



2 (b)

Figure 2

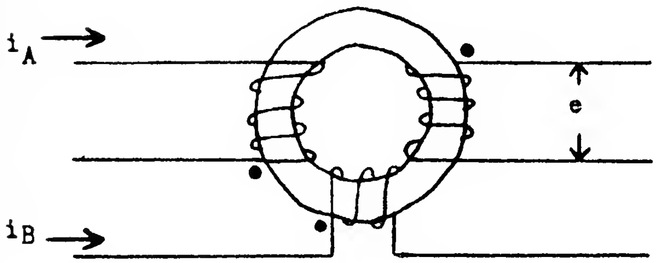


Figure 3

a flux change of $(2B_R + B_A)$. On removal of the applied current the core will remain magnetized in the $-B_R$ or $+ B_R$ state respectively. Since the voltage induced in the secondary winding is a function of the rate of change in flux of the core, it can be seen that a comparatively large voltage will result when the magnetization is switched from $-B_R$ to $+ B_R$ or vice versa, and that a relatively small voltage is induced in the output winding when the magnetization returns to the same state.

The bistable states can be used to represent the binary digits such that when a "ONE" is stored the core is at $+ B_R$ and when a "ZERO" is stored the core is at $-B_R$. Once brought to either state, the core remains polarized, or retains that data, until a force is applied to change it to the opposite state. Thus the core statically stores information indefinitely, unlike the vacuum tube flip-flop whose dynamically stored information is lost as soon as the power is removed.

CHAPTER III

THEORY AND CHARACTERISTICS OF MAGNETIC CORES IN SHIFT REGISTER APPLICATIONS

A somehwat more detailed and complete explanation of core operation in a shift register will be undertaken in this chapter.

1. General Core Operation.

The basic core, described earlier, has a third winding added for shift register applications, as shown in Figure 3. There is, then, an input winding, an output winding and the shift drive winding. The polarities of the windings are such that a positive pulse at the input winding leaves the core magnetized positively, that is, at the positive residual flux state corresponding to a "ONE", while a positive pulse at the shift drive winding leaves the core magnetized at the negative residual flux state, corresponding to the binary digit "ZERO". The polarity of the output winding is such that the shift pulse induces a positive voltage output while the input pulse induces a negative voltage output. In operation as a shift register unit, therefore, the shift pulses are applied periodically, while the input pulses furnish the information to be stored. If no input pulse is furnished the shift pulse maintains the core in its ZERO state, merely traversing the hysteresis loop along the horizontal path to the negative saturation point during the pulse and returning to the

negative remanence point after completion of the pulse. The small change of flux involved in this traversal induces a small voltage signal in the output. If, then, an input pulse is applied, between shift pulses, the core will be switched to the positive saturation point and will return to the positive remanent flux position after the input pulse, leaving a ONE registered. The following shift pulse then switches the core from the positive to the negative remanant flux position, through a considerably greater flux change and thus induces a larger voltage in the output winding.

The presence of a large positive voltage at the output then indicates the core contained a ONE, while a small voltage (or, ideally, no voltage) indicates the presence of a ZERO. However, the information held by the core prior to the application of the shift pulse is lost unless it is utilized at the output or is replaced at the input. This then indicates that perhaps one core can be used to furnish the input to another core such that the large ONE voltage output switches the next core to its ONE state while the smaller ZERO output corresponds to no input to the next core. In this way a magnetic core register is built up, with the input being furnished to one end of the register, digit by digit, as the shift pulses shift the information along the register to fill it. When the information is required, the shift pulses are again applied, and the digits are shifted through the register and appear at the output in the form of "pulse" or "no pulse" of voltage.

There are many complications, not appearing in this simplified description, that affect the performance and circuitry of the shift register:

(a) The negative pulse induced in the output due to an input signal must be prevented from affecting the state of the following core.

(b) The core must be completely switched within the duration of the pulse from the preceding core.

(c) Back flow of information to the preceding core from a voltage induced in the input winding due to the shift pulse must be prevented.

(d) The input and shift pulses must be separated in time since their effects are opposite and if coincident would result in cancellation.

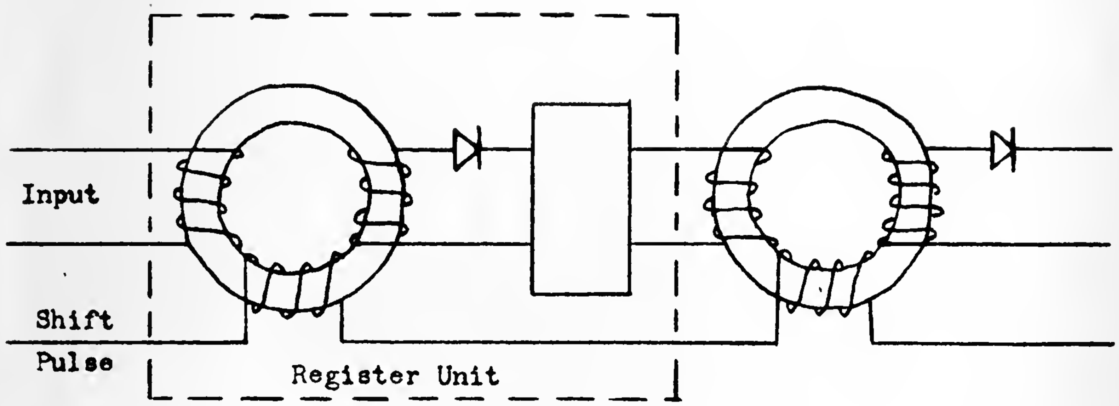
(e) There must be sufficient gain from unit to unit to prevent gradual loss of a ONE and yet not so much gain that a ZERO will be built up into a ONE.

(f) A desirable feature is a low impedance load on the output winding, since, then, fewer turns in the winding would be required and the major item of expense would be reduced.

Methods used to overcome these complications will be discussed in the following paragraphs.

The first item mentioned above, (a), from the first shift register models up to present designs, has been removed by placing a diode in the output circuit. However, in latest designs this diode forward resistance has become the primary factor in item (f). Production of gold-bond diodes with extremely low forward resistance, on the order of 5 ohms, has helped considerably, but the necessity of making the load such that the diode resistance is a negligible portion of the total load still presents an appreciable load to the output winding. No acceptable substitute for the diode has yet proved effective, though the use of the non-linear characteristics of ferrites themselves are under study.

The widely used method of insuring complete switching of the core on application of an input pulse, item (b), is the use of a 2:1 turns ratio of output winding to input winding. An Wang has shown this 2:1 ratio to be the optimum turns ratio to be used, and it has been verified by Sands and also by Sims using slightly different but somewhat idealized approaches. Experiment has also borne out this necessity of a turns ratio greater than one to insure complete switching of the following core and to compensate for the losses in the circuit. Item (e) is also provided by this step up turns ratio.



General Magnetic Core Shift Register Unit

Figure 4

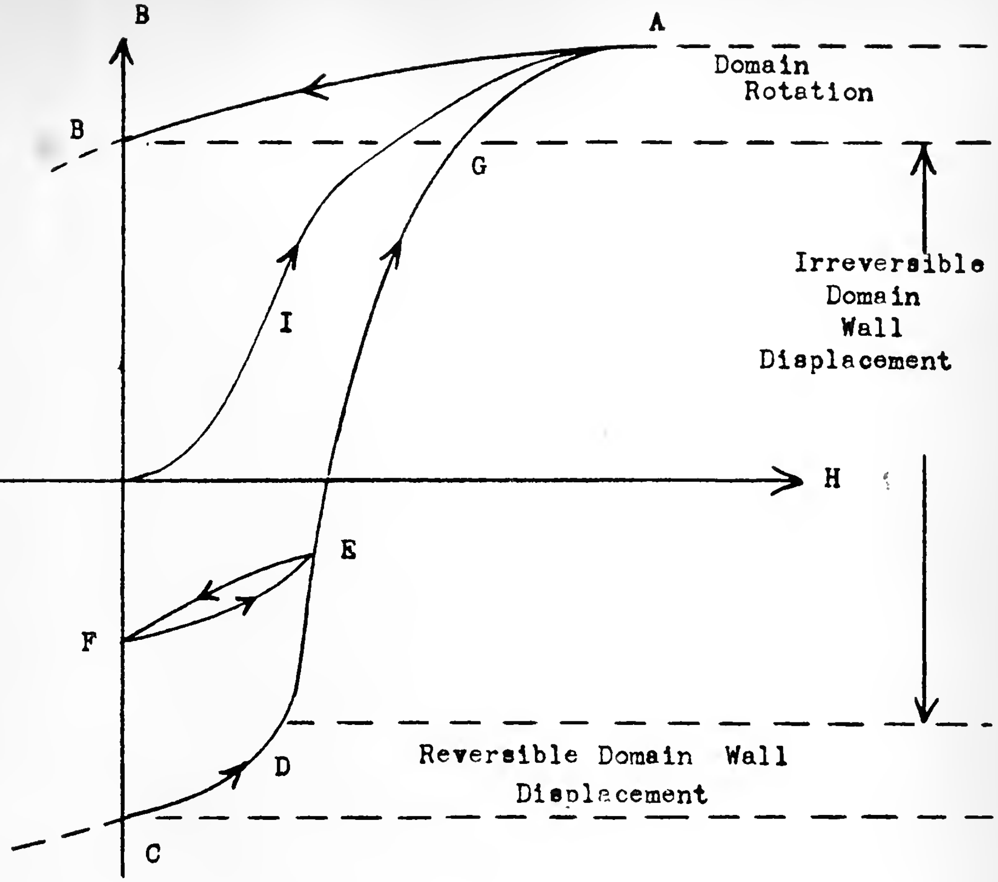
The prevention of back-flow of information and the separation of shift and input pulses, items (c) and (d) were accomplished in some of the first register designs by utilizing two cores per bit of information with two alternately pulsed shift drive lines, each driving alternate cores. Shunt diodes across the input winding and the step-down ratio in the reverse direction also played a part in preventing backflow of information. These registers used the second core as a buffer to store the information until the following core had been cleared. Later designs utilized one core per bit but included a delay section between cores to separate the shift and input pulse effects. Some of these later designs also omitted the input shunt diode and depended solely on the turns ratio to counteract back-flow of information. Observations of some of these later designs are covered in Chapter V.

The problems of design of shift register units have been discussed in the literature. The design criteria in each case serve as directions in which to work rather than as specific design equations due to the necessary approximations used in approaching the problem.

2. Core Behavior

A brief description of the physical behavior of the magnetic core will be undertaken in order to better understand the performance and requirements of the shift register units [9,11].

The phenomena of magnetism results from uncompensated electron spin axes in the atom, and the energy of the exchange force. The exchange force is a function of the orbital energy levels of the uncompensated electron spins, and a certain relationship is required, as is indicated by the non-magnetic character of certain elements which feature uncompensated electron spin, but do not possess the required exchange force. Experimental results indicate the presence, in ferromagnetic materials, of domains within each of which the electron spin axes are parallel, and each domain is thus saturated and possesses magnetic poles. Several domains may exist within a single crystal, and if the resultant magnetic moment of all the domains is zero, the crystal possess no magnetic characteristics, but if the resultant is not zero the crystal exhibits magnetic properties. If undisturbed, the spin axes inherently align themselves parallel to an axis, of easy magnetization, often determined by certain crystollographic axis, due to what is known as anisotropy energy. Depending on the material, there may be one or more than one axis of easy magnetization, and parallel to any one of these axes there may be some electron spin axes aligned in one direction, and some in the opposite, thus, the possibility of many domains within the single crystal. In polycrystalline materials the randomness of the crystal arrangement, each crystal of which can contain several



Magnetization: $I_s = \frac{B}{4\pi}$

Figure 5

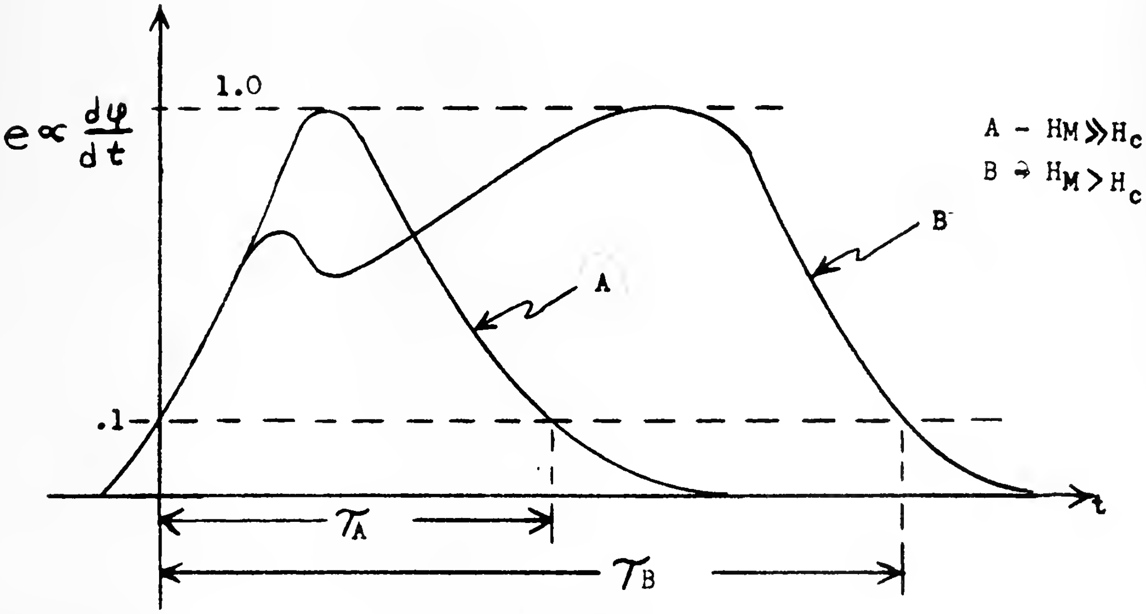


Figure 6

domains, may result in a zero resultant magnetic moment. Closure domains, in which the magnetic moments of adjacent domains close on themselves about a nucleus also result in a zero resultant magnetic moment. Referring to figure 5, a portion of a hysteresis loop, the position of zero resultant magnetic moment is obviously the origin. If a positive magnetizing field is applied, the magnetization of the material follows the path I, resulting in a flux change. This flux change results from the motion of the domain walls which surround a domain and separate each domain from adjacent ones which have different magnetic moments. The wall is of finite depth since the change of direction of spin axis is not an abrupt or step change from one domain to the next. When a magnetizing field is applied, the domains tend to align themselves with this field and as two domains become parallel, the wall between them dissolves and they join into a single domain. As the field is increased more domains align themselves with the field and the domain wall moves with a certain velocity depending on the rate at which these domains become parallel. At low field strengths the domains will assume a magnetization along the axis of easy magnetization in the same general direction as that of the applied field but this may not be parallel to the applied field. This phase of the magnetization is by domain wall motion or domain growth and includes a reversal of many

domains. At higher field strengths, the magnetization of the domains will further tend to align themselves with the field, rotating away from the axis of easy magnetization. Under this condition, magnetization has reached the saturation point, A, in Figure 5. Further increase in the field results in no further magnetization. If the field is now removed, those domains which were rotated will return to the axis of easy magnetization accompanied by a small reversal of flux change and the material rests at point B, the point of residual magnetization, or, correspondingly, for an applied field of opposite polarity, at point C. From this point, if, again, a positive field is applied, the path from C to D is followed, the flux change being due to minor domain wall motion. This motion is reversible, that is, the walls will return to their original positions if the field is removed, due to impeding inclusions, in much the same way a rubber ball tends to move back away from a stone against which it is being pressed, if the force is removed. In this region none of the domain wall motion is due to domain reversal, or shift to other axes of easy magnetization, since then the motion would be irreversible. This region is thus labeled "Reversible Domain Wall Displacement". As the applied field is increased, domain wall motion is due to reversal of domain magnetization and hence is irreversible. This region from D to G, is, therefore, labeled "Irreversible Domain Wall Displacement". However, the presence of irregulari-

ties, or inclusions in the material means that throughout the domain wall motion there is a degree of reversible wall displacement as shown at point E. If the field is removed, the reversal of the wall motion results in a negative flux change and the material ssumes the magnetic state F. It is prevented from returning to C by the irreversible motion in the region D to E. When the field is applied again, energy is expended in the reversible motion as indicated by the different path from F to E, but none of the irreversible domain formation was affected as indicated by the return to the same point E before further irreversible motion begins. At point G all domain magnetization has reversed so that its polarity is generally in the same direction as the applied field, but is parallel to axes of easy magnetization rather than parallel to the applied field. From G to A, the field strength is increased sufficiently to rotate the direction of domain magnetization away from the easy axes and parallel to the applied field as mentioned earlier. This region is thus labeled "Domain Rotation", and is reversible.

It can be seen that, if, in a given sample, an axis of easy magnetization of all of the crystals, or grains, could be aligned parallel to each other and the field applied parallel to this common axis there would be no rotation of domains at high field strengths. This would result in an almost ideal square-loop

and the saturation flux density would be equal to the remanent flux density. This fact has been shown to be true experimentally with a single large crystal. This same effect can be and is obtained to some degree by grain orientation, magnetic anneal or application of stresses to the material.

It has been mentioned that the flux change is a result of the domain wall motion, and when this material is a core with a winding for applying the field, and an output winding, the output voltage is a function of the rate of flux change and therefore of domain wall velocity, or perhaps more closely to the domain wall area. Thus, under an applied field, as the domains increase in size the domain wall area increases, as does the voltage output, until the domain walls begin colliding and dissolving and the wall area starts decreasing, then the output voltage begins to fall. The general shape of the voltage output pulse can thus be seen to increase to a maximum and then gradually decrease to zero. If a field only slightly greater than the coercive force is applied, the output voltage exhibits a double maxima, the first resulting from the reversible wall motion and the second, or major, maximum resulting from irreversible wall growth. As the strength of the applied field is increased the second maximum occurs earlier until it completely obscures the first maximum. This is the normal condition of operation in shift register ap-

plications, that is, the applied field is sufficiently strong that the output voltage reaches a single maximum and then decays.

The time required for the core to complete its domain wall motion on application of a magnetization force is called the "switching time", τ, and is taken as the time between the 10% amplitude points of the output voltage waveform, as shown in figure 6. The switching time has been found to be inversely proportioned to the applied field, in accordance with the expression: $(H_m - H_o)\tau = S_w$. Where H_m is the applied field, H_o is the threshold field for irreversible domain wall motion corresponding to point D in figure 5, and Sw is the switching coefficient. Sw is a constant for applied fields such that $H > 2H_c$ if the rise time of the applied field is less than the switching time. This relationship is shown in figure 7, and can be seen more clearly if the above expression is rewritten in the form $H_m = S_w \cdot \frac{1}{\tau} + Ho$ which is the equation of a straight line of slope Sw and intercept Ho.

The switching coefficient consists of two factors: $S_w = S_w^e + S_w^r$ where Sw^e is the contribution due to eddy current effects and Sw^r is the contribution due to relaxation effects. The relaxation effects arise from delay of the electron spin axes in aligning themselves with an applied force and is an inherent characteristic of the material. The eddy current effects are negligible in ferrite due to the high resistivities of the material, and can be made negligible in metal cores by proper

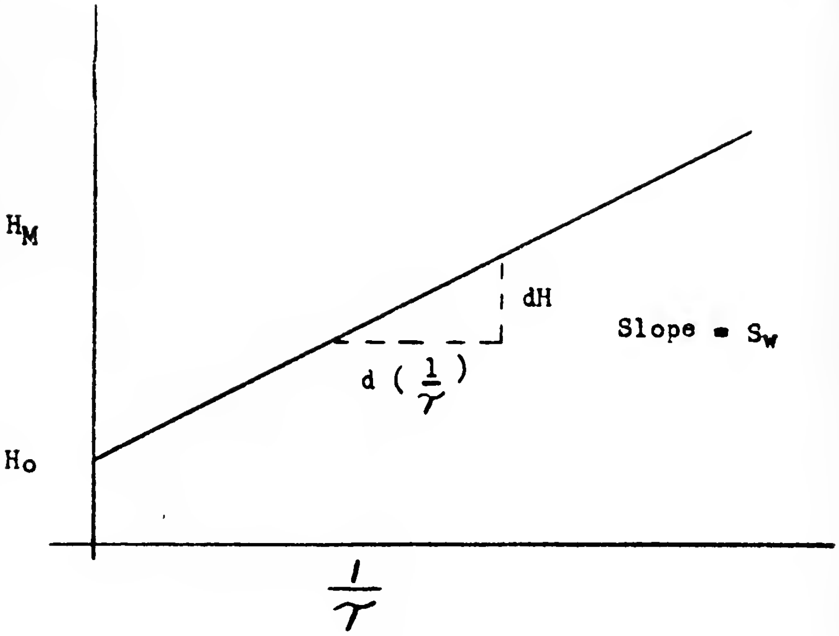
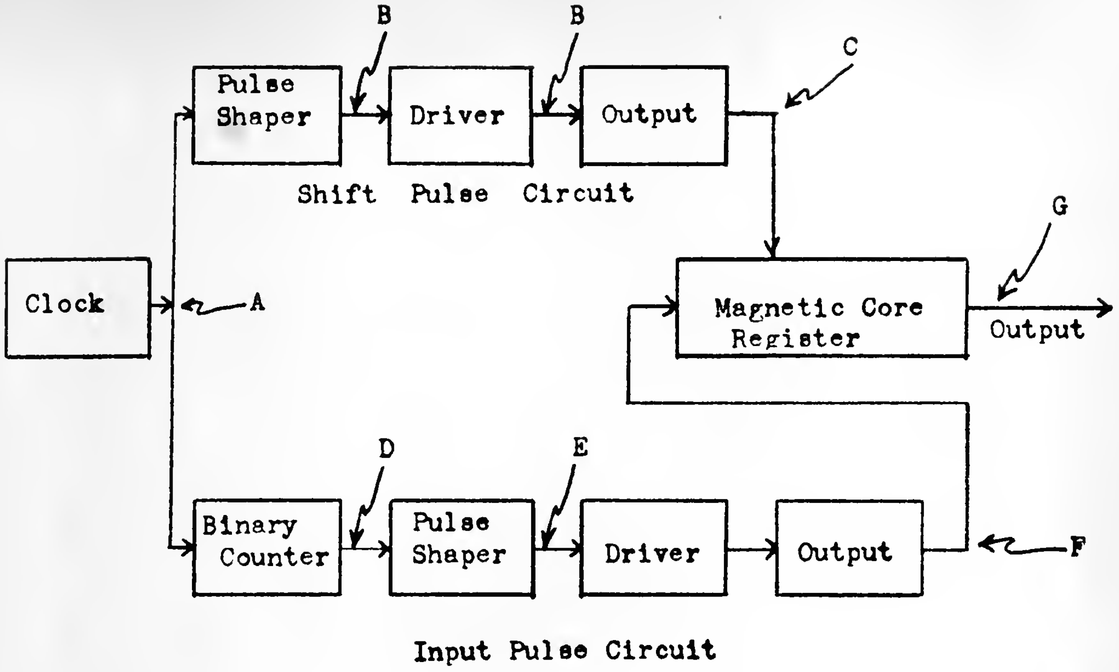


Figure 7

treatment of the material, primarily by using sufficiently thin tapes in winding the cores.

Heating in the cores are a result of the eddy current losses, relaxation losses and the hysteresis losses. The eddy current losses can again be made negligible as above, while the relaxation losses are directly proportional to the applied field. The effects of the heating are to cause increased random motion of the atoms of the material and thus increase the difficulty of domain formation and axes alignment. At the Curie temperature this motion becomes completely random and the material loses its magnetic properties. This then places a limit on the conditions under which the material is used and is much more critical in ferrite cores than in metal cores since in the ferrites the internally generated heat cannot be conducted to the core surface and removed by external cooling. A high Curie temperature is thus desirable since it permits more flexible operating conditions. Since Sw^r is inversely proportional to the Curie temperature, a high Curie point will also result in shorter switching times and in lower heating loss.

Many of these points will be recalled in Chapter V in explaining the effects observed in operating the core register units.


B
B
C
Pulse Shaper
Driver
Output
Shift Pulse Circuit
G
Clock
A
Magnetic Core Register
Output
D
E
Binary Counter
Pulse Shaper
Driver
Output
F
Input Pulse Circuit

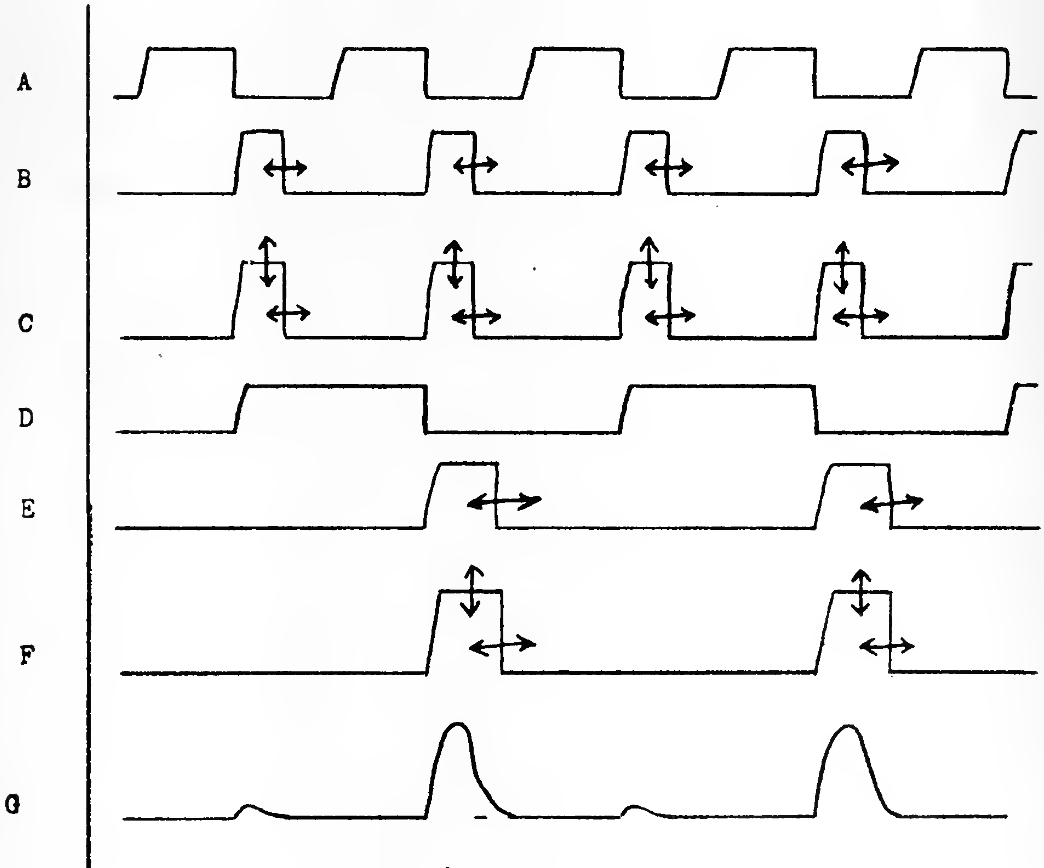

A
B
C
D
E
F
G

Figure 8

CHAPTER IV

EQUIPMENT ARRANGEMENT FOR OBSERVATION OF REGISTER OPERATION AND CORE PERFORMANCE

The tests and observations were performed in the laboratories of National Cash Register Company, Electronics Division. It was therefore desirable and time-saving to utilize as many of that company's existing and standard circuits as possible in the test set-up, making modifications where necessary to meet varied requirements.

The block diagram of the equipment arrangement is shown in figure 8.

The clock circuit used was an available free-running multivibrator designed for 100kc operation. This circuit was modified to provide for a variable frequency range of approximately 50kc to 500kc. The clock served as the trigger source for both the shift pulse line and the input pulse line.

The circuitry used to obtain a shift pulse consisted of a "one shot" multivibrator pulse shaper circuit, modified to furnish a variable pulse width over the range .4 to 3 μsec. This pulse was amplified in the driver to furnish sufficient drive to the 6CD6 output stage. The amplitude of the output pulse was made variable over the range of about 120-540 ma, depending to some degree on the load which the magnetic core shift register presented

to the stage. The load of the output stage consisted of the shift windings of all the units being tested in series in the plate circuit.

In arriving at the circuitry for the input pulse, it was desirable to furnish some sort of characteristic logical input in order to simulate an actual computer input to the register. The first block in this circuitry thus was a four stage binary counter, modified to count 10 and reset in order to correspond with the number of units in the register being tested. The counter was also modified to increase the frequency range at which it was capable of operating satisfactorily. However, without extensive modification, the counter circuit set the upper limit of 250kc at which the tests were conducted. The output of the counter was shaped by another "one shot" multivibrator circuit, modified to furnish a variable input pulse width of 1 to 4 μsec. This pulse was then amplified and used to drive the cathode follower output stage, where the amplitude of the input pulse could be varied over a range of 4- 60 ma. The input winding of the first register unit was inserted in the cathode circuit as the load.

This test set up then furnishes the following variable

1. Shift Pulse	Width	.4-3 µsec
	Amplititude	120-540 ma
2. Input Pulse	Width	1 - 4 µsec
	Amplititude	4 - 60 ma

3. Operating Frequency: 50 - 250 Kc.

In addition, the 10 digit word pattern from the counter could be set up to furnish any arrangement of ONEs and ZEROs desired.

In retrospect, it would have been informative to have been able to vary the rise and fall times of the shift pulse to permit observation of the effects on register performance and individual core behavior.

CHAPTER V

OBSERVATIONS OF COMMERCIALLY AVAILABLE REGISTER UNITS

Four commercial magnetic core shift register units were available, three of these in sufficient number to permit testing as a register system. The fourth type was represented by a single unit which was used solely for study of circuit arrangement and design.

The four types of units will be designated A, B, C and D throughout the remainder of this chapter. Types A, B and C were set up as registers and tested at the maximum attainable frequency, with the shift and input pulse variables adjusted for optimum performance as determined by the signal to noise ratio. The frequency used in Registers A and C was 250 Kcs as limited by the equipment, while Register B operation was limited to 100 Kcs by the register characteristics.

The characteristics and circuitry of the four units are presented in Section 1 together with the general observations of Registers A, B and C. Section 2 contains more specific observations of a single register under more detailed tests. Conclusions concerning core unit operation based on the observations make up Section 3.

1. General Characteristics.

The requirements of the circuit surrounding a core when used in a shift register were discussed in Chapter III. Briefly, these requirements were: input, output and shift windings and a non-linear coupling device between cores. The units of primary interest to the writer were the single-core-per-bit units, since they are in the best position to compete economically with other types of registers and delay lines. The major expense in core units is the winding cost and this is obviously reduced where one core is used instead of two. Another advantage of single core units is in the requirement of a single shift source which brings about an improvement in both cost and reliability. Thus, only single-core-per-bit register units are included in this study.

Figure 9 gives the circuitry and manufacturer's characteristics of Register Unit A, while figure 10 shows the wave forms at various points of the unit while operating at 250 Kcs. The voltage waveform across the input capacitor to the delay line was used in the tests of all units as the indicator for optimum performance, that is, signal to noise ratio, since, in use, it is this signal that would be used as the output from a complete register. The component values of Unit A were calculated from indirect measurements and hence may be in error. No winding information was obtained

and no data on core material was available, however, it is believed that the core is similar to that in Units B and D.

Figures 11 and 12 give the corresponding information for Unit B, except that the operating frequency was limited to 100 Kcs. At higher frequencies the period did not permit the information pulse (Terminals 6 - 9) to decay to the point where it would not interfere with the following bit.

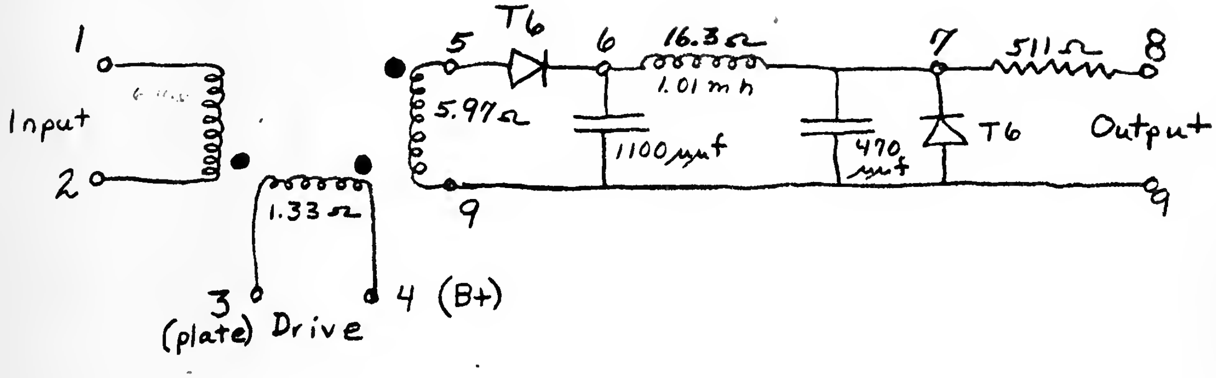
Similar information is given for Unit C in figures 13 and 14. Here, again, the operating frequency is 250 Kcs, the upper limit of reliable performance for the test equipment and not the upper frequency limit for the units, either in this case or that of Unit A. The circuit and manufacturer's characteristics only are given for Unit D in Figure 15. No tests were made on the single unit of this type, however, the indicated component values were obtained by measurement. It is interesting to note that the output/input winding turns ratio used is half the theoretical optimum of 2:1 as indicated in Chapter III.

2. Specific Observations.

Several tests were made on a register consisting of 10 units of Type A, in order, first, to become familiar with operation of the core units, and then to obtain data on operating limits and effects of change in the variables: shift pulse duration and amplitude, input pulse duration and amplitude and frequency.

UNIT A

Manufacturer: Epsco, Incorporated.
Model   : S R 200

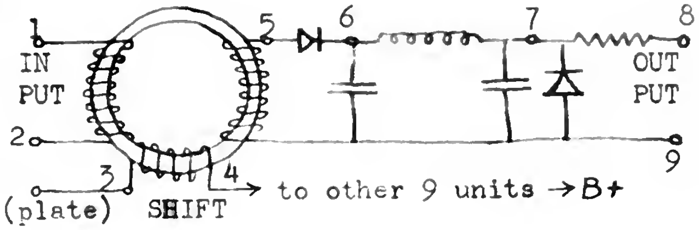


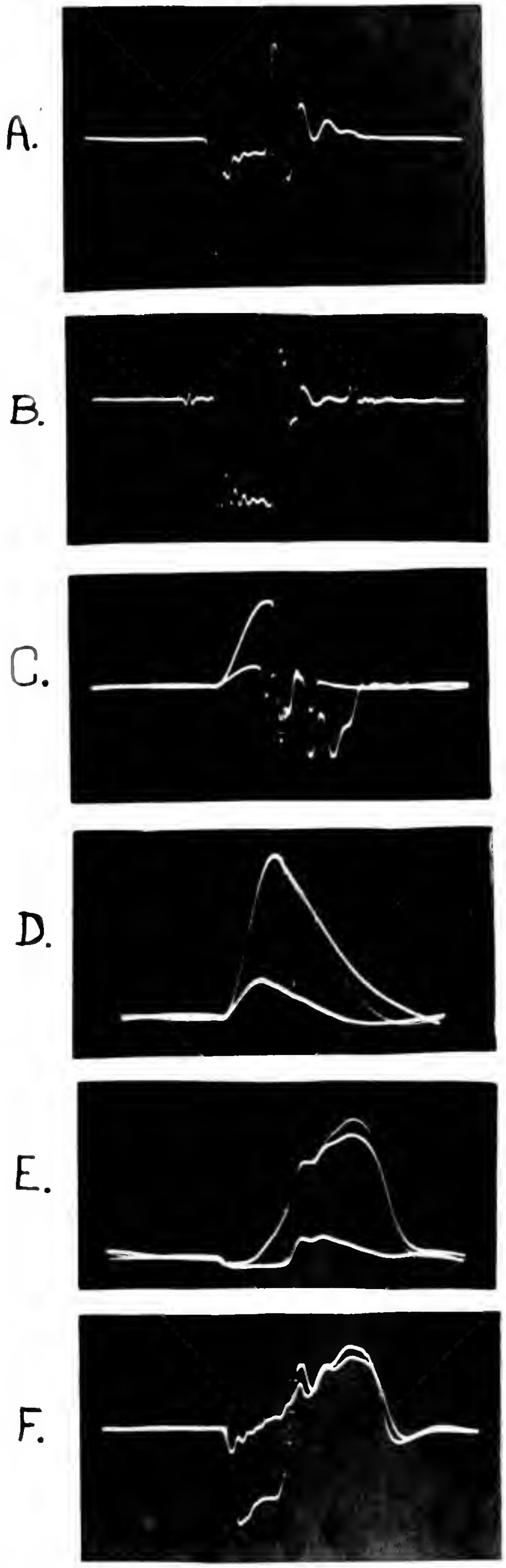
Manufacturer's Typical Characteristics:

Shift Pulse:	Amplitude:	300 ma
	Width:	0.5 to 1.5 μsec
Input Pulse:	Amplitude:	15 volts
Information Rate:	200 Kc	Design Center
	350 Kc	Maximum
Peak Power per Shifted One at Design Center:	1.4 watts	
Winding Data:	None	
Core Data:	None	

Figure 9

MAGNETIC CORE UNIT "A"





WAVEFORMS:

Frequency: 250 Kcs
Horizontal Scale: 0.5 u-sec/div

A. Shift Pulse Voltage (10 units)
Terminals: 3 - 4
Vert. Scale: 25 volt/div

B. Shift Pulse Current (Inverted)
Terminals: 4 - gnd (across 10 Ω)
Vert. Scale: 100 ma/div

C. Core Output Voltage
Terminals: 5 - 9
Vert. Scale: 5 volt/div

D. Capacitor Voltage
Terminals: 6 - 9
Vert. Scale: 2.5 volt/div

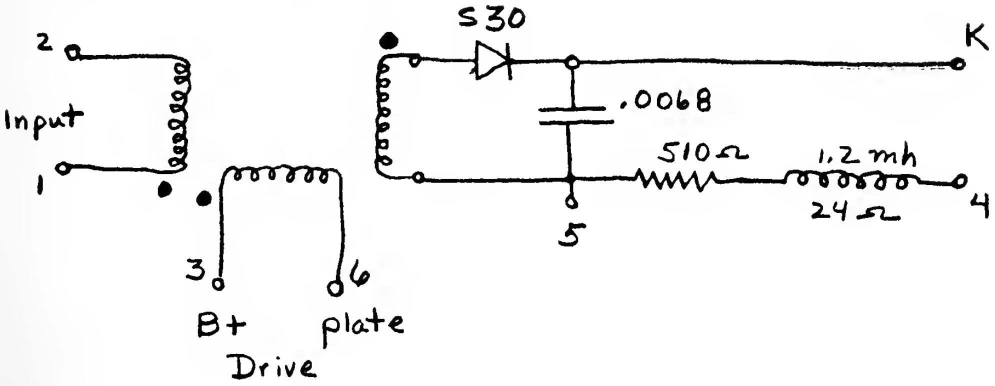
E. Diode Voltage
Terminals: 7 - 9
Vert. Scale: 2.5 volt/div

F. Output Voltage to Next Core
Terminals: 8 - 9
Vert. Scale: 3 volt/div

FIGURE 10

UNIT B

Manufacturer: Raytheon
Model: S R - 100



Manufacturer's Typical Characteristics:

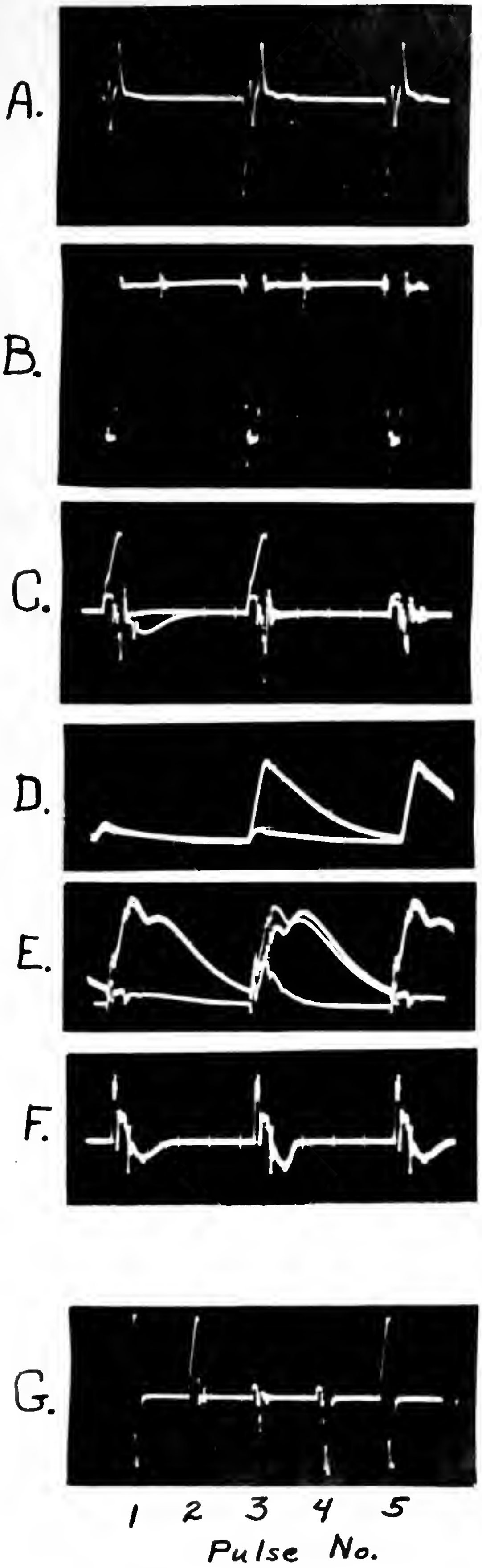
Shift Pulse:	Amplitude	225 ma
	Width	2.2 μsec
	Rise time	.25 μsec
	Fall time	.40 μsec
	Volt drop	8 v per ONE
		2 v per ZERO
Input pulse:	Amplitude	10 - 20 ma
	Width	5 μsec
Information Rate:	0 to 100 Kc.	
Power dissipation:	.25 watts per ONE at 100 Kc	

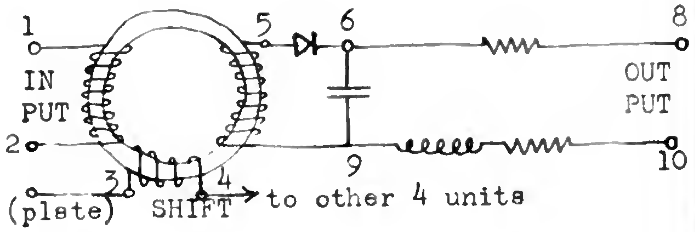
Winding Data: None

Core Data: Ribbon wound
5/16 in. I.D.
1/8 in. wide

Figure 11

MAGNETIC CORE UNIT "B"





WAVEFORMS:

Frequency: 100 kcs
Horizontal Scale: 2 u-sec/div

A. Shift Pulse Voltage (5 units)
Terminals: 3 - 4
Vert. Scale: 50 volt/div

B. Shift Pulse Current (Inverted)
Terminals: 4 - gnd (across 10 ohms)
Vert. Scale: 100 ma/div

C. Core Output Voltage
Terminals: 5 - 9
Vert. Scale: 10 volt/div

D. Capacitor Voltage
Terminals: 6 - 9
Vert. Scale: 10 volt/div

E. Current Output to Next Core
Terminals: 6 - 8
Vert. Scale: 10 ma/div

F. Voltage Output to Next Core (Inverted
Terminals: 8 - 10
Vert. Scale: 10 volt/div

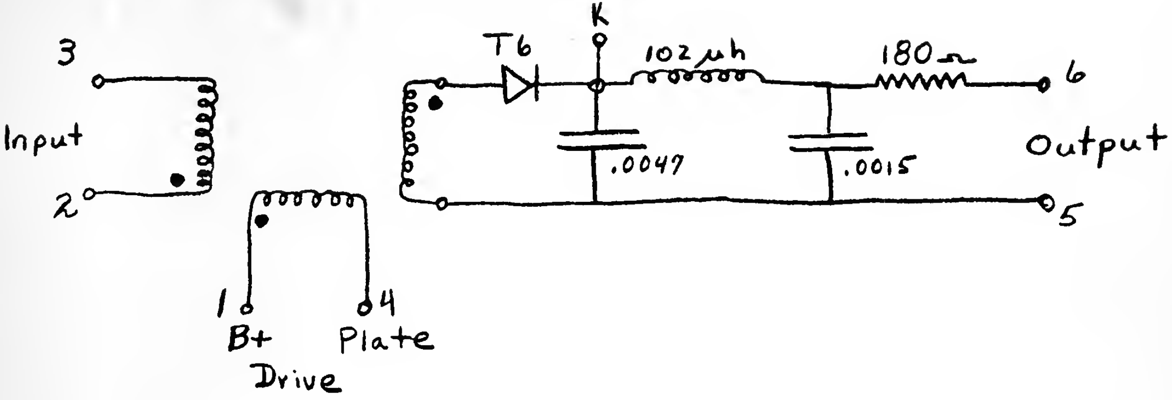
G. Core Output Voltage
Terminals: 5 - 9
Horiz. Scale: 4.5 u-sec/div
Vert. Scale: 10 volt/div
Pulse Schedule:

Pulse No.	Core Input	Core Output
1	ONE	ONE
2	ZERO	ONE
3	ZERO	ZERO
4	ONE	ZERO
5	ONE	ONE

FIGURE 12

UNIT C

Manufacturer:	Raytheon
Model:	S R 500



Manufacturer's Typical Characteristics:

Shift Pulse:	Amplitude	300 ma	
	Width	0.5 μsec	
	Rise Time	0.1 μsec	
	Fall Time	0.2 μsec	
	Volt Drop	10 v per ONE 2 v per ZERO	
Input Pulse	Amplitude	40 ma	16 ma
	Width	1 μsec	10 μsec
Information Rate:	0 to 500 Kc		
Power Dissipation:	3 watts peak per transfer .5 watts at 500 Kc for all ONEs.		

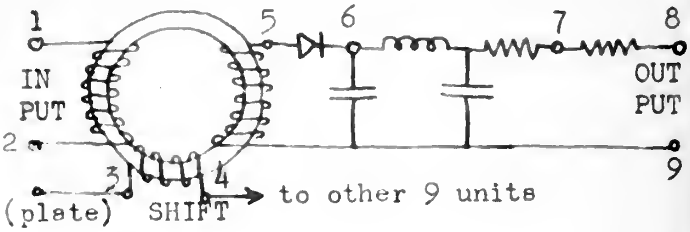
Winding data:	Input Winding	19 turns
	Output Winding	36 turns
	Shift Winding	27 turns

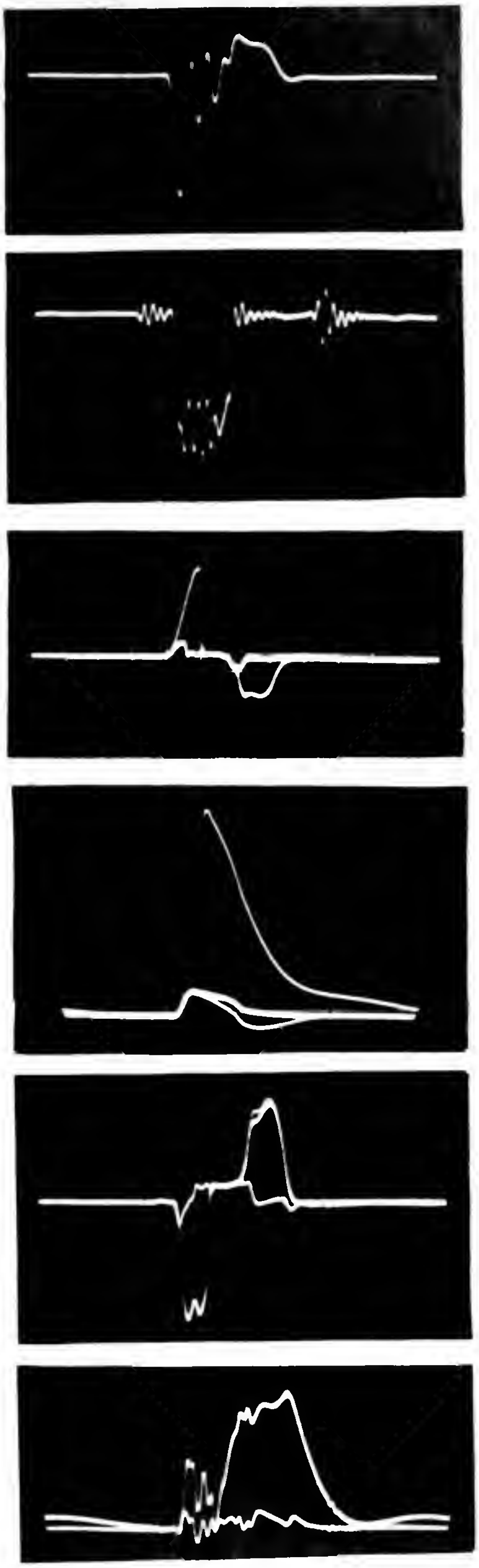
Core data:

Ribbon Wound
1/8" I.D.
1/16" Width
.5 mil thick
11.5 turns
4.5 in. ribbon length

Figure 13

MAGNETIC CORE UNIT "C"





WAVEFORMS:

Frequency: 250 kcs
Horizontal Scale: 0.5 u-sec/div

A. Shift Pulse Voltage (10 units)
Terminals: 3 - 4
Vert. Scale: 25 volt/div

B. Shift Pulse Current (Inverted)
Terminals: 4 - gnd (across 10 ohms)
Vert. Scale: 100 ma/div

C. Core Output Voltage
Terminals: 5 - 9
Vert. Scale: 5 volt/div

D. Capacitor Voltage
Terminals: 6 - 9
Vert. Scale: 2 volt/div

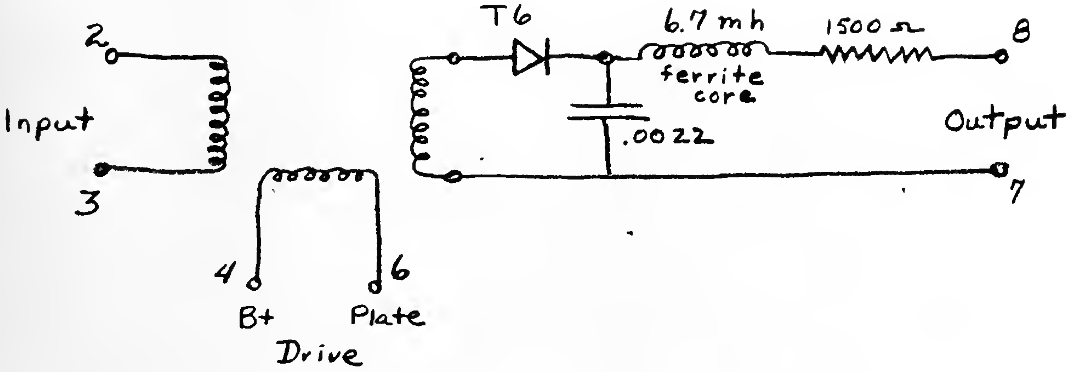
E. Output Voltage to Next Core
Terminals: 8 - 9
Vert. Scale: 1 volt/div

F. Output Current to Next Core
Terminals: 7 - 8
Vert. Scale: 10 ma/div

FIGURE 14

UNIT D

Manufacturer: Sprague Electric
Model: 70Z2



Manufacturer's Typical Characteristics:

Shift Pulse:	Amplitude	180 ma
	Width	2.5 μsec
	Rise Time	1.0 μsec
	Fall Time	0.5 μsec
	Volt drop	20 v
Input Pulse:	Amplitude	15 ma
	Width	3 μsec
Information Rate:	0 to 150 Kc	
Power dissipation:	3.6 watts peak	

Winding Data:	Input winding	101 turns
	Output winding	100 turns
	Shift winding	52 turns
	Ferrite Core Choke	120 turns

Core Data: Ribbon wound
5/16" I.D.
1/8" Width

Figure 15

The primary criteria of performance was the signal-to-noise ratio as determined by the ratio of amplitudes of the smallest ONE to the largest ZERO voltage outputs. The largest ZERO, in all cases, was the first ZERO following a ONE, indicating that the ONEs were not being completely shifted out of the core. That is, the applied field was not of either sufficient amplitude or duration to insure reversal of all the irreversible domains, and the next applied field completed this reversal resulting in sufficient flux change to cause an increased voltage output. An arbitrary lower limit of 6:1 was set for the signal-to-noise ratio below which dependable operation would not be assured. However, Register A operated satisfactorily, for a period of about two hours, with a S/N ratio of 4:1 as seen in Figure 10. It was noted that the ratio of amplitudes of the largest ZERO to smallest ZERO could not exceed 2:1 without these larger ZEROs being amplified to ONEs and consequently loading the register with ONEs.

A distinct decrease in shift pulse amplitude requirements was noted for specific values of shift pulse duration. For the register of Units A, this point occurred at a pulse duration of 0.9 μ-sec and was independent of operating frequency. The decrease was so marked that a distinct saving in power requirements could be made by limiting operation to that re-

gion. It is believed that this performance is a function of the delay network configuration coupled to the output winding, i.e., the natural frequency of the network, perhaps.

It was also noted that current requirements of the input circuit were much lower than those of the shift circuit. This can be explained by considering the applied field in each case. The applied field is directly proportional to the effective current through the windings. Since the shift winding presents a relatively high impedance and the output winding approaches an open circuit to the voltage induced by an input pulse, little current flows in either of these two circuits during the input pulse and the input current is the effective current. However, the output circuit presents a very low impedance and the input winding presents a moderately low impedance to the shift circuit with resulting high currents in each. The effective current during the shift pulse is thus the shift current less the input and output circuit currents and the requirements on the shift circuit are consequently considerably higher.

Variations of input pattern had little or no effect on the register performance for the relatively short periods of operation during these tests. However, since more power is required to switch ONEs than ZEROs, there may be a detrimental effect due to heating if a pattern of predominantly ONEs were being

shifted over long periods of time.

3. Conclusions.

The following conclusions are drawn from the observations made and from theory.

General:

a. A reasonable lower limit for signal-to-noise ratio is 6:1 to insure reliable performance.

b. The maximum operating frequency can be approximated from the reciprocal of the time from the start of the capacitor voltage to the point where the amplitude of the decaying ONE is equal to the maximum ZERO voltage.

For unit A this is 460 Kcs
B this is 125 Kcs
C this is 550 Kcs

Shift Pulse:

a. The shift pulse duration need be no longer than the time required for the output voltage to reach a maximum. The duration is correct for Units A and B, figures 9 and 11, but could be reduced to 0.5 μsec for Unit C, figure 13.

b. There is an optimum point for the shift

pulse amplitude duration relationship. This point reduces requirements of the shift pulse source but is dependent more than likely on the coupling circuitry between cores, specifically the diode and input capacitor, and may thus require more critical selection of diodes.

c. The rise time of the core output voltage pulse is determined by either the shift pulse rise time or the RC time of the delay network input diode and capacitor whichever is longer. The shift pulse rise time should be just slightly shorter than the RC time therefore to reduce the high frequency content of the pulse and thus the eddy current losses.

d. No improvement in performance is obtained by increasing the shift pulse duration/amplitude relation above a satisfactory minimum.

Input Pulse:

a. No improvement in register performance is obtained by increasing the input pulse amplitude or duration above that necessary to reliably write in the information.

CHAPTER VI

PERFORMANCE OF A REGISTER IN A D. C. COUPLED DIGITAL COMPUTER

The requirements and performance of a computer register can best be summarized by discussing an existing register. The adaptation of a magnetic core system as a replacement register will then be discussed. A study has been made of the arrangement of such a replacement register, however, the actual operating register has not been constructed.

1. Characteristics of an Existing Register

The register to be discussed in this section is the magnetic drum system used by the National Cash Register Company in the CRC 102 Digital Computer. This computer has five registers that, basically, operate in the same manner, the differences lying primarily in word length and read-out circuitry. The specific register to be considered here is the E register which, to the writer appears to be the most flexible register and has the most demands placed on it.

The basic register has a storage capacity of 42 bits, the word length used in this machine. Of these, 37 bits are recorded magnetically on the drum and five, the first or lower order bits, are stored in vacuum tube flip flops. External connections to the drum are through read and write heads and

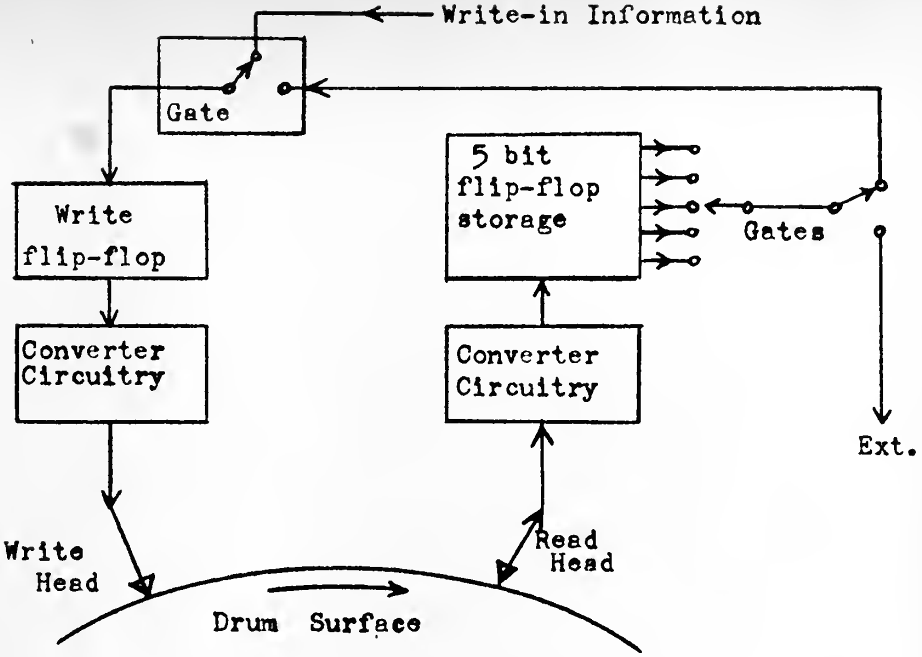


Figure 16

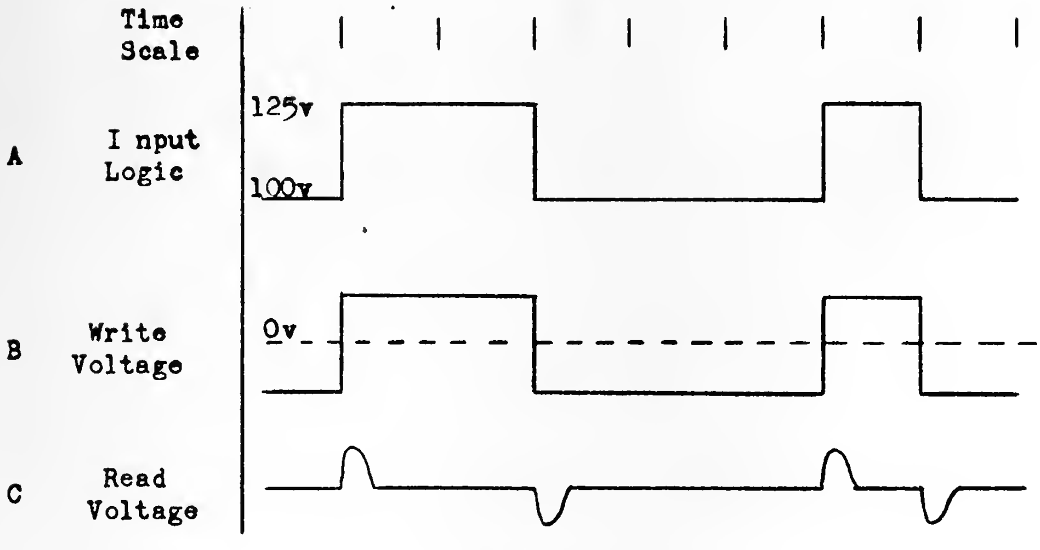


Figure 17

converter circuitry. In block diagram form, the register appears as in figure 16.

In operation, new information is gated into the write circuitry which includes a driver, a flip-flop and a write amplifier. The write amplifier drives the write or record head such that the magnetic surface of the drum is driven to saturation in one polarity for a ONE and in the opposite polarity for a ZERO. The write process thus automatically erases any previously recorded information. The read head is then very accurately set a distance along the drum surface from the write head such that there are 37 bits recorded on the drum. From the read head, the information passis through two stages of preamplification, a phase inverter and a clipper to shape the trigger and to arrive at a proper time sequence for setting the first of five flip-flops, E1 through E5. The output from the register is normally taken from the output of E5, but can be taken, through logic gates, from E_1 through E4 to permit shifting right one to four bits for binary, octal or decimal manipulations or additional flip-flops can be gated on to the output of E5 to permit shifting to the left. The information can also be gated back to the input of the write circuit so that the word can be recirculated through the register. The information can remain in the register by recirculating it at

the same time it is being furnished through the output to an external circuit such as an adder, or another of the registers. The entire operation of the register is on a step basis, rather than a continuous basis, as each bit of information progresses in synchronism with the computer clock. It can be seen that the information is continuously stepping, however, either to the output or through the recirculating circuit. If it is desired to determine the contents of one particular bit in the word it is necessary to wait until that bit is contained in one of the flip-flops and then gate the contents of that flip-flop to an indicator of some sort.

The logical information with which the register is to perform is of the NRZ form, that is, there are two distinct voltage or logical levels, each level representing one of the logical states ONE or ZERO, as shown in Figure 17. This signal, for drum recording must be converted to a similar NRZ form but with the levels symmetrical about zero voltage such that magnetization of the drum surface of either polarity can be achieved. This can be performed quite easily by use of a bias arrangement in the write circuitry.

The output of the read head then must be reconverted to the original logical levels from the form shown in Figure 17 C. This is accomplished through amplification, clipping

and inverting before applying the signal to the flip-flop stages.

The requirements of a register can then be summarized as follows:

1. Information handling rate of the register must be synchronized with the rest of the machine both as to bit stepping and to word timing.
2. Register must be capable of accepting, at the input, the logical information in the form in which the remainder of the machine handles it, and must furnish at the output the identical form, and information content.
3. Reliability must be high, requiring, primarily, that the number of vacuum tubes used be a minimum.
4. Cost of the register must be as low as is consistent with speed and reliability.
5. Register must be flexible enough to perform the required operations; storage, furnish output while storing, shift right or shift left. (Storage in the drum register is obtained by recirculation).
6. In some cases, it is necessary to be able to examine the contents of one or more bits

in the register as an indicator of state of the solution of a problem, next step to be taken by the computer, etc.

CHAPTER VII

UTILIZATION OF MAGNETIC CORE REGISTERS IN A D.C. COUPLED COMPUTER

The proposed methods of meeting the requirements of register performance, stated in the previous chapter, with a magnetic core register will be discussed from the points of view of the input requirements and general circuitry, the output requirements and general circuitry and the shift pulse requirements and general circuitry. This will be followed by a general statement of operating conditions and recommendations.

1. Input Requirements and General Circuitry.

The input to the register is of the NRZ form as mentioned previously, while within the magnetic core register the information is of the pulse, or return-to -zero form. Thus, the input circuitry must be capable of converting the NRZ input to a pulse form of information. This information is of binary form, that is, only two states exist, either ONE or ZERO.

a. One method of signal conversion would thus be to let a pulse represent ONE and no-pulse represent a ZERO within the register. Conversion of the input information to this form can be accomplished relatively simply by differentiating the logical product of the input information and the clock signal and utilizing each fall pulse to trigger the register input circuit. A suitable input drive circuit in this case would be

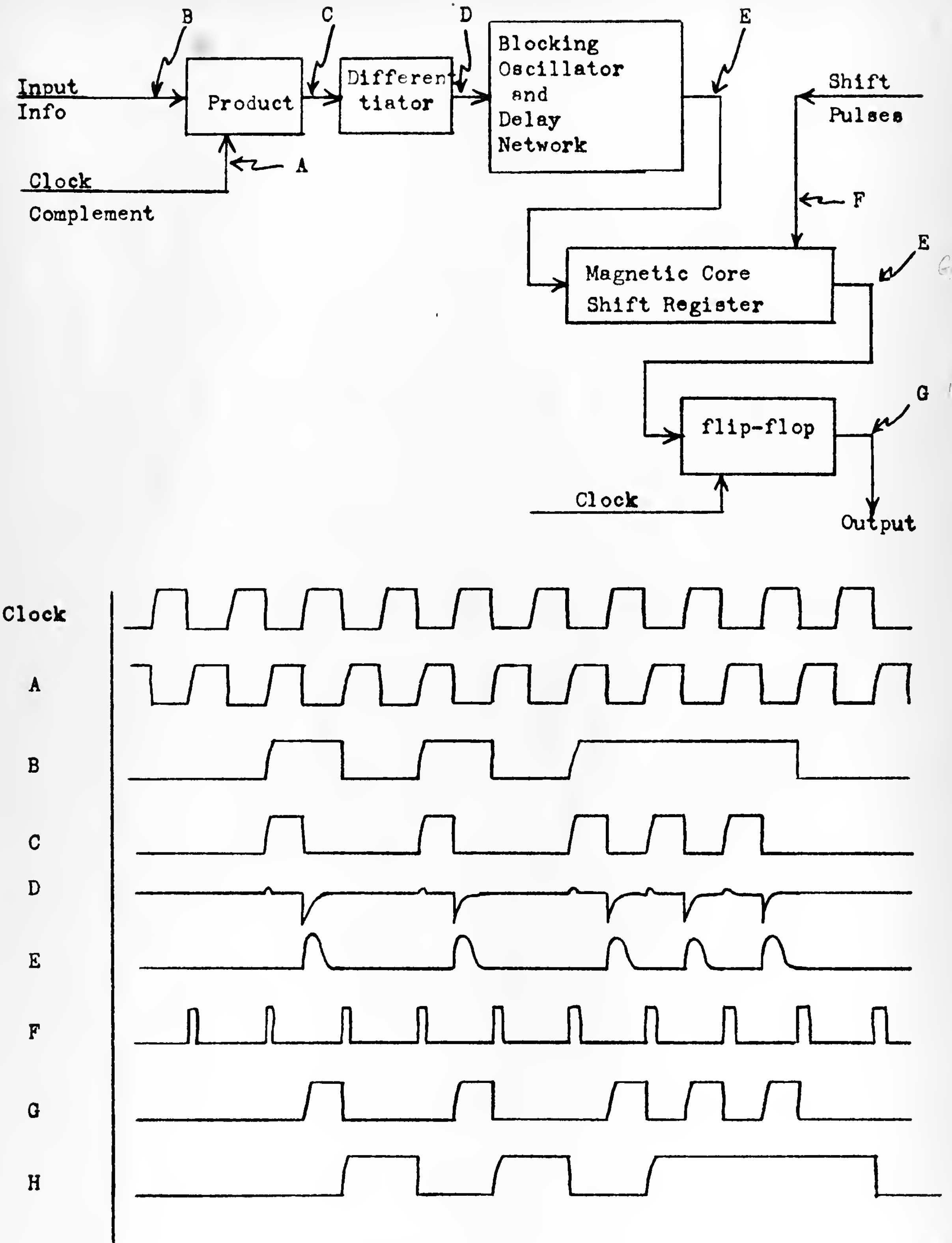
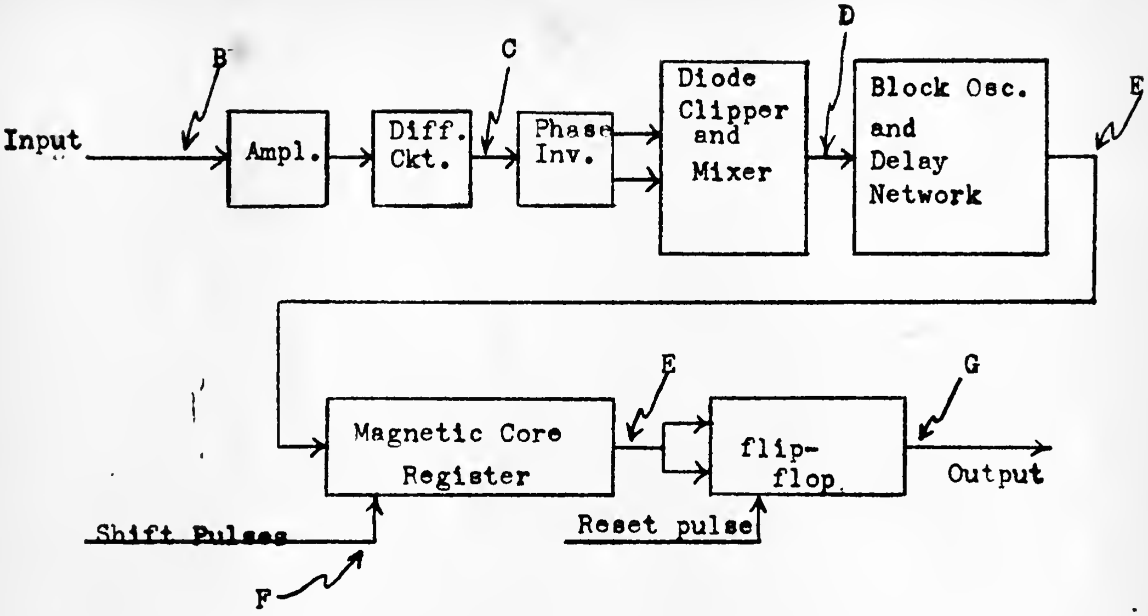

B
C
D
E
Input Info
Product
Differentiator
Blocking Oscillator and Delay Network
Shift Pulses
A
Clock Complement
F
Magnetic Core Shift Register
E
G
flip-flop
Clock
Output
Clock
A
B
C
D
E
F
G
H

Figure 18

a blocking oscillator with the input trigger applied to the plate of the oscillator with the input trigger applied to the plate of the oscillator and the output taken from the cathode circuit. A block diagram of such a circuit is shown in Figure 18, with the approximate waveforms at the indicated points. It is evident that a delay must be introduced in the input pulse sequence so that the input pulse and the shift pulse will not be applied to the core at the same time and thus interfere with the proper switching of the core. This delay can be introduced at the output of the blocking oscillator through use of a pi section filter of the form used between the magnetic core units as shown in Figure 9 or 13. Another source of delay would be to use the fall of the clock complement instead of the clock to trigger the blocking oscillator. This latter method is considered the better by the writer, and is shown in Figure 18, since it introduces a positive fixed delay and insures the necessary time separation between input and shift pulses. If the clock complement is not available, however, the filter type delay network must be used.

b. A second method of signal conversion would be to furnish an input pulse to the register only when a change in logical level occurs, that is, when the logical state changes from ONE to ZERO or from ZERO to ONE. In this case, the product term is not required, the necessary triggers for the pulse forming circuit being obtained directly from the input information by a differentiating network. The trigger pulses thus occur at both the rise and the fall of the input information. Since the remainder of the machine performance is based on the fall of the waveform, it is of reasonably good shape from which to derive a trigger pulse. However, the rise time may have deteriorated, particularly at the output of a logical network, due to multiple time constants, to the point where it does not lend itself to use as a suitable triggering source. The poor rise time can be overcome either by amplifying the input signal so that only a small, and hence, reasonably sharp, part of the rising signal is used, or the input information can be used to set a flip-flop which furnishes good rise and fall times at the output. If the output of such a flip-flop


Input
B
Ampl.
Diff.
Ckt.
C
Phase
Inv.
Diode
Clipper
and
Mixer
D
Block Osc.
and
Delay
Network
E
Magnetic Core
Register
E
flip-
flop
G
Output
Shift Pulses
F
Reset pulse

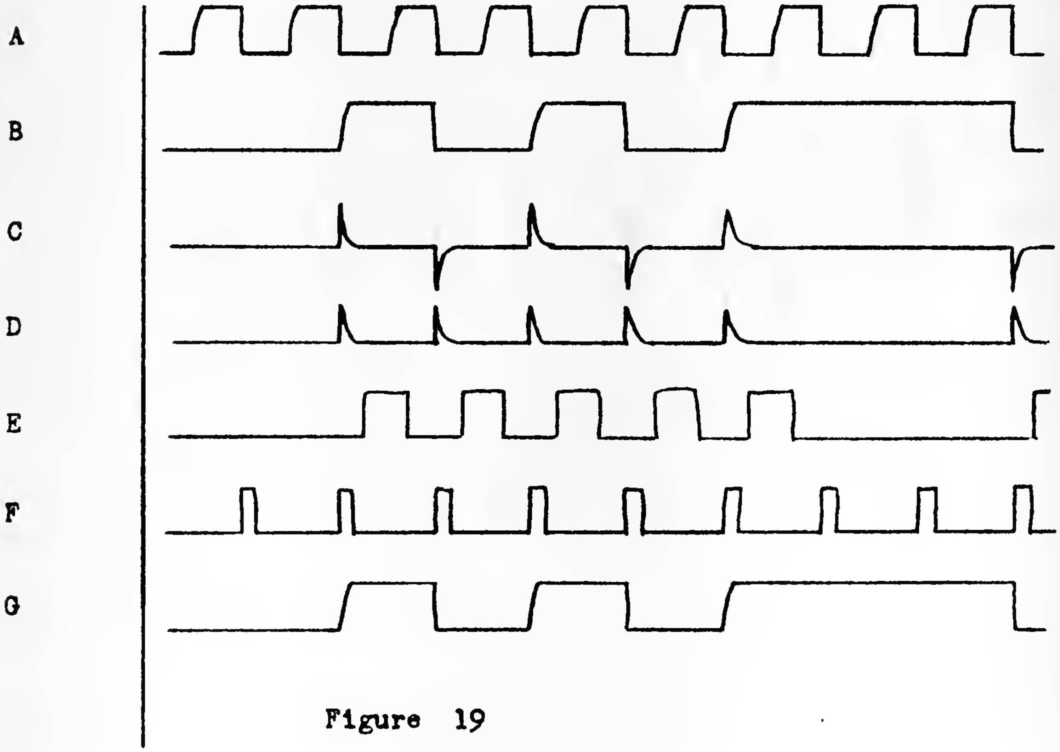

A
B
C
D
E
F
G

Figure 19

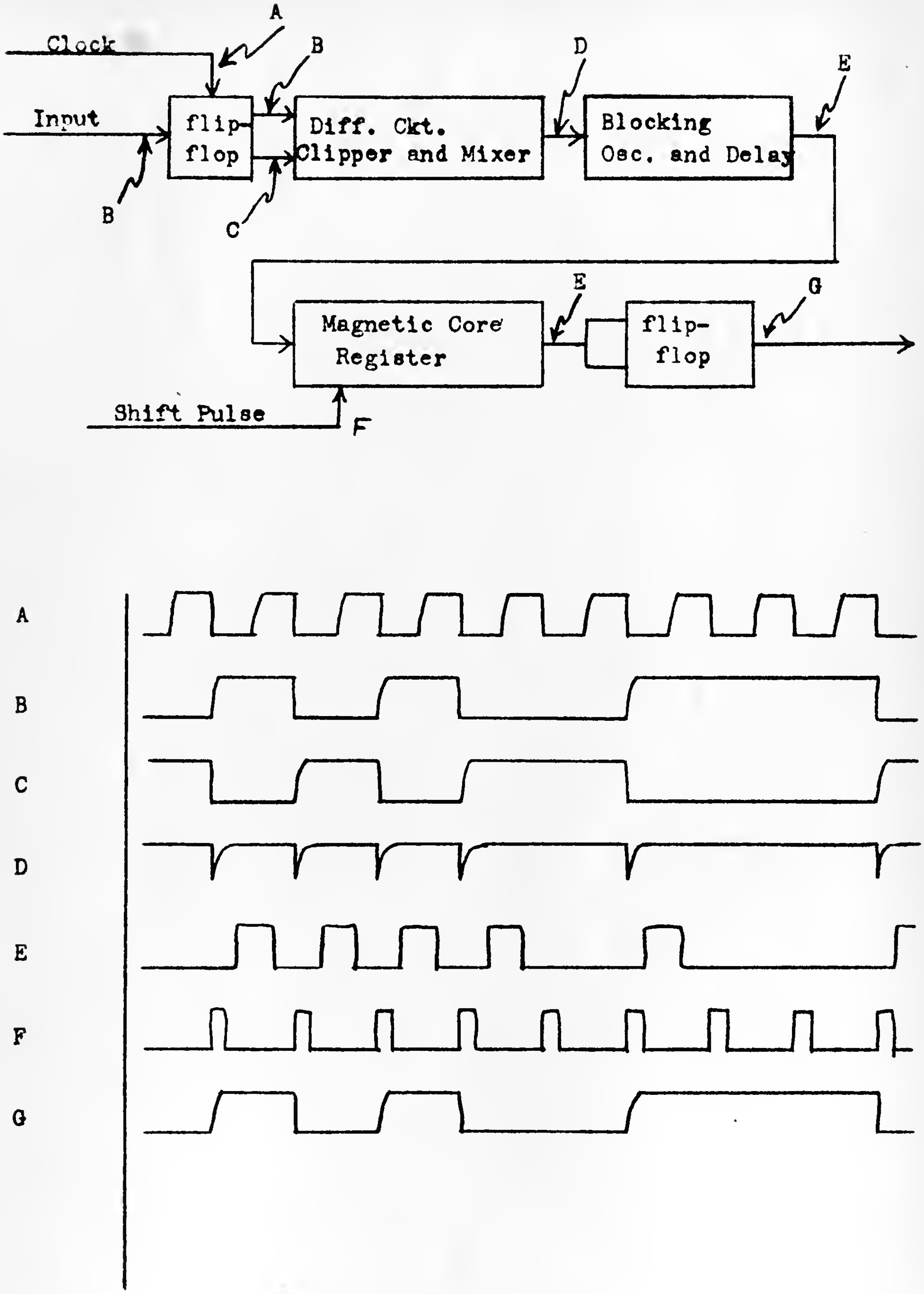

A
Clock
B
D
E
Input
flip-flop
Diff. Ckt. Clipper and Mixer
Blocking Osc. and Delay
B
C
E
G
Magnetic Core Register
flip-flop
Shift Pulse
F
A
B
C
D
E
F
G

Figure 20

is used the rise trigger could also be obtained from the fall of the input complement and the fall trigger obtained from the input information as before. However, the use of the flip-flop inherently introduces a delay of one clock period in the signal transmission which may or may not be permissible in a specific application. These two systems are shown in block diagram form in Figures 19 and 20 respectively, together with the pertinent wave forms.

The input amplifier circuit is preferred by the writer since it does not involve the loss of the clock period. The output of the amplifier is differentiated and applied to a phase inverter and diode clipper circuit so that the input to the grid of the biased "one shot" blocking oscillator is a series of positive triggers. The output of the blocking oscillator is again taken from the cathode through a filter type delay network which is necessary in this case since the input pulse and the shift pulse are triggered at the same time.

The performance of the flip-flop input circuit is similar to that of method (a) above, following the mixer circuit, with the exception that, again, a delay must be introduced as in the amplifier circuit above.

A variety of input circuits have thus far been presented.

Selection of any one of them will depend in part on the remaining register circuitry and so will be left to Section 4, after variations of the other circuits have been discussed.

2. Output Requirements and General Circuitry.

The output circuitry must be capable of reliably converting the pulse form of information from the register to the NRZ form for external use. The most logical circuit for this application is a vacuum tube flip-flop which is triggered to the proper state by the pulse output from the register. However, the pulse information, as determined in the previous section, might be of either of two forms:

(a) a pulse corresponding to and occuring for each ONE, with no-pulse for a ZERO.

(b) a pulse for each change in logical level, that is a change from ZERO to ONE, or from ONE to ZERO.

The same flip-flop circuit can be utilized in either case, the only variation required being in the triggering circuitry.

In information of type(a), the output from the register is used directly to trigger the flip-flop to the ONE state, while each clock pulse is applied to return the flip-flop to the zero state at the end of each clock period. Thus the output from the flip-flop is a series of distince ONE's for a pattern of the form "1111" instead of remaining in the ONE

state through such a pattern, however, the desired information remains the same. The block diagram and waveforms for this method are included in Figure 18. A flip-flop following the one whown will then reproduce the information in the original form as it appeared at the input as shown in H, Figure 18. A diode logical network following the flip-flop shown will preserve the half-period ONEs as shown at G, with no detriment to information manipulation, however.

The output flip-flop is again triggered directly by the pulses of form (b), but in this case, both flip-flop inputs are triggered by the same pulse. This pulse, being positive, for example, will trigger the "off"-side of the flip-flop to the "on" state, but will not affect the "on" side. The flip-flop must be reset to the proper state at the start, prior to shifting a word into it from the register to insure that the flip-flop output contains the input information, and not the complement of that information. The block diagram and waveforms for this circuit are shown in Figure 19 and 20 with the assumption that the flip-flop has been reset to ZERO. In either of these two circuits, Figures 19 and 20, the information is seen to spread over into the next clock period, but for information manipulation the last half of the information signal is the significant part so that this "slopping" over will have no ill effects.

3. Shift Pulse Requirements and Circuitry.

Outside of the actual core unit circuitry, the magnetic core register depends more heavily on the shift pulse characteristics than any other thing. These characteristics were discussed generally in Chapter V and will not be repeated here. However, it will be recalled that the energy dissipated by the core units is a function of the shift pulse amplitude, duration and shape, or perhaps, more loosely, the duty cycle. Since the pulse characteristics are quite well prescribed, within limits, by the units in use, other methods of reducing the duty cycly of core operation were sought.

The shift pulses can be applied continuously, as triggered by every clock pulse, to the core register, so that the information is being continuously shifted through the register, as in the magnetic drum system. Storage is then obtained by recirculation, which requires the cores to operate at a maximum continuous duty cycle, and the static storage capabilities of the cores are not used. The facilities for shift right or shift left would also have to duplicate, somewhat, that of the drum system, that is, fill out a portion of the register word length with flip-flops in order that the output may be taken from other than the 42nd bit storage unit. It is not felt that sufficient reliability would be attained in gating the core outputs directly to obtain the shift

right-shift left flexibility, and if, for example, the five low order units were paralled with output stages, then it would be advantageous to remove those five low order core units and replace them directly with vacuum tube flip-flop circuits. Thus, there are several disadvantages to a system in which the shift pulses are applied continuously.

A more promising system appears to be one in which the shift pulses are applied only when required either to furnish an output from the register, or to recirculate the register contents once in order to determine the information content of one particular bit. In this way the core unit duty cycle is held to a minimum resulting in less core heating and therefore improved reliability. This system thus will be discussed more fully as to the circuits required, beginning with the shift pulse output stage.

An average current pulse amplitude of approximately 250 ma. is required of the shift pulse to switch the core units, and the voltage drop across each shift winding is approximately 10 volts. A fairly heavy-duty beam-power tube thus appears to be the most suitable output tube in order to permit operation well within the tube's dissipation ratings for increased reliability and to permit driving a maximum number of core units per output stage, so that fewer output stages are required.

For example, with a 42 bit word length, three output tubes of type 6CU6 or 6CD6 can each handle, quite easily, 14 core units, with a total plate voltage drop of about 140 volts during the shift pulse. The stages are biased beyond cutoff so that the quiescent current is negligible to prevent placing a bias on the cores which would interfere with the information transfer through the input windings. The peak current amplitude of the shift pulse should be adjustable at each stage and can be easily controlled by a variable potential divider in the screen supply. Grid clipping at the input of each output stage can be used to improve the input pulse form, to reduce loading on the driver stage, and also to insure a more uniform pulse amplitude at the output of the three stages.

The shift pulse driver is thus required to furnish a signal of approximately 100 volts at a low impedance level to the output stage. A suitable driver circuit to satisfy these requirements is the blocking oscillator with the output taken from the cathode. The input to the driver stage is obtained from the differentiated output of a gating circuit.

The trigger input to the gating circuit is the clock pulse since it is necessary to synchronize the shift pulse with the clock. The enabling input to the gating circuit is obtained from the output of a flip-flop, such that when this enabling flip-flop is set to one state, the clock pulses will pass through

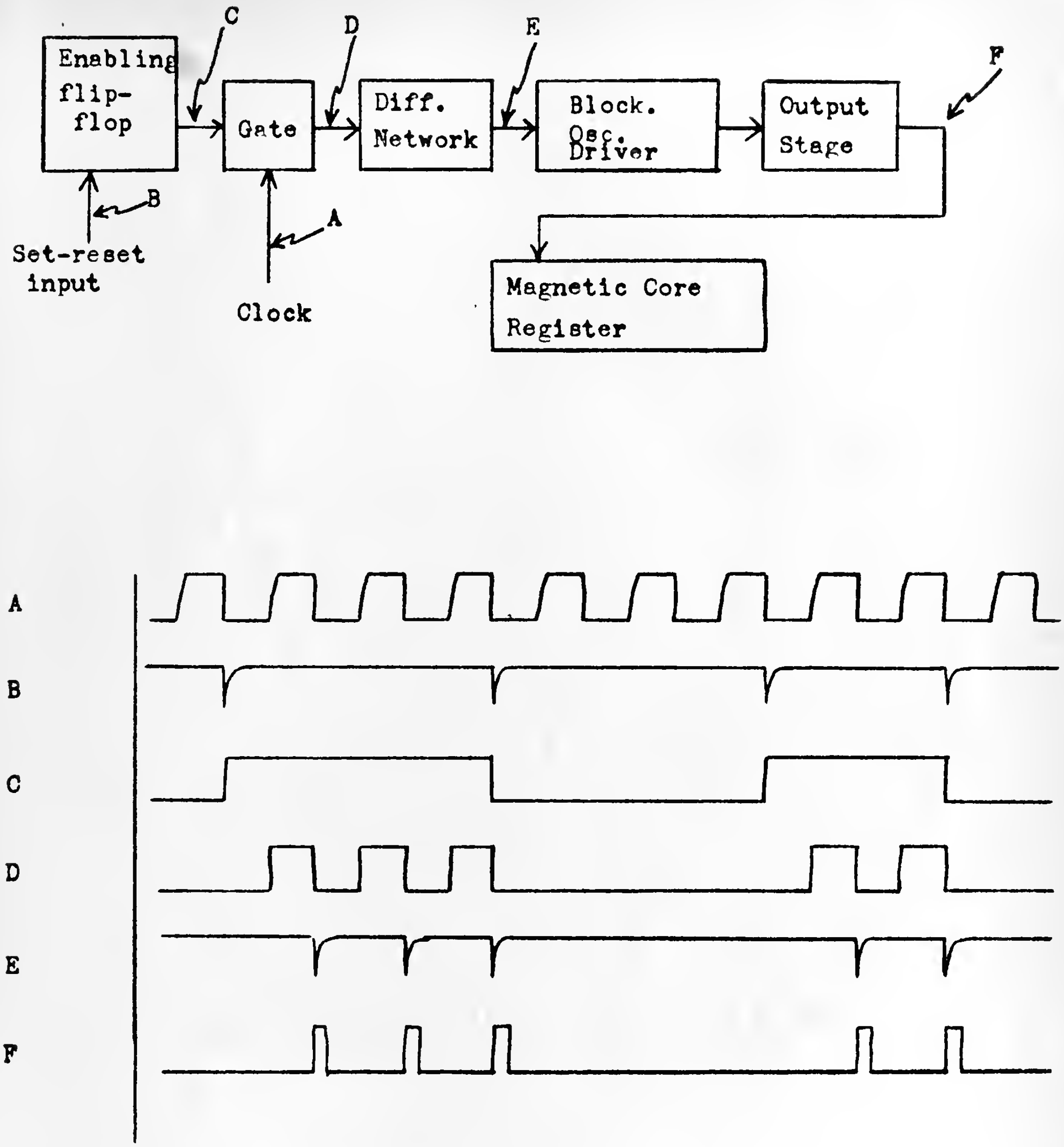

Enabling flip-flop
Gate
Diff. Network
Block. Osc. Driver
Output Stage
Magnetic Core Register
Set-reset input
Clock
A
B
C
D
E
F

Figure 21

to trigger the shift pulse circuit and the contents of the register are shifted through bit by bit. When the enabling flip-flop is set to the opposite state, the clock pulses are prevented from passing through the gate to trigger the shift pulse circuit. The enabling flip-flop input is obtained from logical networks which will control the start and stop of the shift pulse train as follows:

(a) For normal operation, the shift pulses start at initial word time and stop after one word period, that is, 42 bits.

(b) To shift right, the shift pulse train starts the required number of bits early, for example, to shift one octal digit to the right, the shift train will start 3 bits ahead of the initial word time.

(c) To shift left, the operation will be similar to (b) above, but the shift train will start late by the required number of clock periods.

(d) To recirculate one word, the operation will be identical to (a) above, the recirculation being a function of the output logic network.

A block diagram of the shift pulse circuitry is shown in Figure 21 with the pertinent wave forms. This system does not require the additional stages at the register output that were

needed to permit right and left shifts in the first system mentioned above and in the drum system discussed in Chapter VI.

4. The Complete Magnetic Core Register System.

The only shift pulse circuit considered for a complete register system is the enabled system since it offers distinct advantages by way of reduced duty cycle for core units and shift circuitry and reduced complexity and number of vacuum tube stages in the output circuit.

For the input-output circuitry, methods (a) as shown in Figure 18 would not operate when required to recirculate, without incorporating an intervening flip-flop with resulting loss of one clock period, since the output pulse and the clock complement occur in alternate half periods and thus could not be gated to furnish the input trigger. If the input information is gated with the clock pulse, and the necessary delay obtained in the output of the blocking oscillator, this circuit and the circuit of Figure 19 are identical in performance characteristics. Since neither circuit has a duty cycle advantage over the other, there is no distinct preference for one over the other. Experience with actual performance of both circuits might however, lead to a preference for one. The circuit of Figure 20 is not considered due to the undesirable loss of one clock period.

Referring now to the requirements for register performance at the end of Chapter VI, the magnetic core register has been shown to be capable of handling in the form in which it is used by the remainder of the machine, that is, the NRZ form. The control circuitry in connection with the register lends to it the required flexibility to permit storage, shifting right or left, and recirculation. The register speed is the same as the remainder of the machine since the shift pulse is trigered from the same timing source. Circuit selection will permit operation over the same word period, also, without loss of a clock period. Thus the magnetic core register, including the associated circuitry, is capable of satisfying the performance requirements of a computer register. More specific conclusions regarding the replacement of existing drum recirculating registers are drawn in Chapter VIII.

5. Other Applications of Magnetic Core Units.

Much work is being conducted toward the application of magnetic core logic circuits, and in the combining of magnetic core and transistor circuits in an attempt to attain higher degrees of reliability in computer performance.

Another application similar to that discussed in this paper in circuitry and operation is in the tape recorder used in conjunction with the computer. At present a vacuum-tube flip-flop buffer line is used to accept and store information from the

computer at a high information rate and then release this information at a much lower frequency to the recorder circuits to be recorded on the tape. The buffer also serves to accept information from the tape recorder and transfer it to the computer input circuitry. The magnetic core unit is particularly well adapted to this application since all that is required is to gate into the shift pulse circuitry the proper trigger frequency and to gate the input and output to the required circuits. The distinct advantages to be gained through use of the magnetic core system in this application are reduced cost, reduced size, reduced power requirements, reduced heating and static storage.

CHAPTER VIII

CONCLUSIONS

The magnetic core register with the associated circuitry has been developed in block diagram form to enable this register to perform the operations required of an existing register. Specific circuit design depends to a large degree on the circuit characteristics of the remainder of the computer. Thus the performance characteristics of the magnetic core register are capable of successfully competing with those of other systems in use, specifically, the magnetic drum system.

The wide range of satisfactory shift pulse and input pulse characteristics insure reliable performance as regards both effect of component change and accuracy of transmitted information. Reliability is also improved through the use of fewer vacuum tube stages, a weak member in itself, by reducing the heating effect on adjacent components. An approximate comparison of the number of vacuum tube stages includes 11 stages in the magnetic core system versus 19 in the magnetic drum system. However, this difference in number is countered somewhat by the fact that conditions under which some of the magnetic core stages operate do not lend themselves particularly well to long tube life.

Only a very approximate comparison of costs of a magnetic

core register versus a magnetic drum register can be drawn due to the limited core designs presently available. It is felt that an average cost of five dollars a unit is well within reason for production units in their essential form and not encased. (One commercial unit is available at this time at an approximate cost of $3.50 per unit in large lots.) The writer obtained eight dollars per stage as an estimate of the cost of vacuum tube circuits; that is, for the two stages in a flip-flop circuit, the cost for a suitable unit is sixteen dollars. The cost of the drum is neglected for that system since the drum is present for other purposes, however, the cost of recording heads is approximately two hundred dollars each. Thus, an approximate cost comparison is three hundred dollars for a 42 bit magnetic core register versus five to six hundred dollars for an equivalent magnetic drum register.

Space requirements cannot be compared since they depend entirely on the final form which the magnetic core units would take. However, it is estimated that space requirements would be about equal for the two systems.

Summarizing, it is felt that the advantages to be gained through use of the magnetic core register are great enough to warrant their use in future equipments but not great enough to warrant replacement in existing machines.

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Thesis 29748
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